Some examples of SPICE compact modeling for design of advanced analog integrated circuits in CEA-Leti

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http://www.dese.iisc.ernet.in/ifwdm/
Materials Properties

- "Physics" & Backgrounds
  - Gate stack (atomistic approach)
  - Quantum transport (NEGF, Wigner)
  - Mobility (MC, Kubo-Greenwood)

Devices Characteristics

- TCAD
  - Process
  - Devices
  - Small circuits (ring oscillator, SRAM, etc.)

IC Performances

- SPICE for circuit design
  - Compact Modeling
  - Parameter extraction

Leti experimental data
Technological & Nano-Characterization platforms

- Improving "Physics" understanding
- Technological support (choice of technological options, device optimization, ...)
- Performance evaluation (from device to IC)
- New ideas or concepts, innovation (challenge anticipation)
Main application fields

**Memories**
- Split-Gate
- Resistive RAM (OxRAM, CBRAM)
- Phase Change Memory
  - Physics/TCAD/SPICE

**Advanced CMOS**
- Silicon platform
- FDSOI
- 3D integration
- Nanowire
- Carbon based electronics
  - Physics/TCAD/SPICE

**RF**
- Active and Passive
  - Physics & SPICE

**Photonics**
- Back-end applications (wave-guide)
  - SPICE

**Power devices**
- III-V on silicon
- Automotive & Photovoltaic applications
  - TCAD/SPICE

**Photovoltaic**
- Multi-crystalline silicon
- Hetero-junctions
- Nanodots
  - Physics/TCAD
1 - MOSFET compact modeling for design of mixed analog/digital circuits at cryogenic temperature
(MOS-AK workshop*, Rome, Italy, 2010)

2 - HSP: A surface-potential-based compact model of AlGaN/GaN HEMTs power transistors
(MOS-AK workshop, Bordeaux, France, 2012)

3 - Development of Verilog-A models for silicon photonics devices and implementation in a standard EDA environment
(MOS-AK workshop, London, UK, 2014)

* http://mos-ak.org/

Other examples: MOS-AK workshop, Grenoble, March 12, 2015
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1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

Why cryogenically cooled CMOS?

- 40°C
- 125°C
77 K LN₂
4.2 K L⁴He
200 K
300 K
100 K
0 K

Dry ice

- Room Temperature

Read-out circuits for high performance infrared (IR) imagers
Hybrid circuits (flip-chip)

Automotive electronics & low perf. uncooled IR imagers

0.3 K: far IR detection for astronomy (L³He + L⁴He)

Herschel Space Observatory/PACS (European Space Agency)

3.5 m diameter mirror

1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

CMOS cooled at Ultra Low Temperature (ULT)

- Ariane 5 launch: 14 May 2009
- End of mission: 29 April 2013

- Electrical characterization at 0.3 K and 4.2 K
- Low frequency noise meas. at 4.2 K
- CMOS = PD-SOI severe floating effects (kink)
- Lack of MOSFET model
- No complete parameter extraction
- “Simple” but robust read-out circuit: mainly PMOS source-followers and switches
- 0.5 µm commercial CMOS process

ULT ASIC: 0.3 K stage (from Si bolometer arrays 2560 px)

LT ASIC: 2 K stage

Test module
1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

⇒ CMOS cooled at Low Temperature (77 < T < 200 K)

Many standard effects:

- e.g. standard INW (Inverse Narrow Width) effect in PMOS

- Temperature scaling to be improved for precise analog modeling in a wide range: 77 - 300 K

Some specific effects:

- Anomalous INW effect in NMOS
- Negative gate transconductance Gm at high Vgs
- Degradation of weak inversion slope
- Freeze-out effect in LDD regions
- Energy subbands quantization effect
- Fair agreement obtained with the Hafez model with impact ionization.
- Strong impact of these regions during characterization traditionally made in the linear regime \( (V_{ds} \leq 50 \text{ mV}) \) ⇒ artifacts in \( V_{th} \) \( (L) \) extractions.
1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

⇒ Energy subbands quantization effect

Peak in $G_m$ for moderate inversion, only on lightly doped and long NMOSFET ($< 8 \times 10^{16} \text{ cm}^{-3}$)

⇒ Subbands quantization effect

(Ando, 1982)
1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

Subbands quantization effect: numerical 2D simulations with Atlas (Silvaco)

Poisson-Schrödinger simulations:
- Si (100) ; $m_L=0.916$ $m_0$ ; $m_T=0.19$ $m_0$
- degeneracy: $g_L=2$ ; $g_T=4$
- $N_A=5\times10^{16}$ at/cm$^3$ ; $T=200$ K ; $T_{ox}=3.3$ nm

Occupancy vs Drain current

Occupancy $\Leftrightarrow$ Drain current
dOccupancy/dVgs $\Leftrightarrow$ Gm

1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

Toward compact modeling of the subbands quantization effect

\[ F_s : \text{surface electrical field} \]

\[
E_n = \frac{(q \, \hbar \, F_s)^2}{(2 \, m_{\perp})^{\frac{1}{3}}} \times \text{Ai}_n
\]

\[
N_{n}^{i=L,T} = \frac{g_i \, m_i}{\pi \, \hbar^2} \times kT \, L_n \left[ 1 + \exp \left( \frac{E_F - E_n}{kT} \right) \right]
\]

\[ Q_{\text{inv}} = q \sum_{n=1}^{\infty} N_{n}^{i} \]

\[ Q_{b} = \sqrt{2 \, q \, \varepsilon_{Si} \times N_{\text{ch}} \times (\Phi_s + V_{sb})} \]

\[ F_s = \frac{\eta \, Q_{\text{inv}} + Q_{b}}{\varepsilon_{Si}} \]

Exact \( F_s \) ?

\[ \mu = \mu_0 / \left[ \left( Q_{\text{inv}} / Q_{c} \right) + \left( Q_{c} / Q_{\text{inv}} \right)^{\alpha-2} \right] \]

\[ I_{ds, \text{Lin}} = \frac{W}{L} \times V_{ds} \left( \mu_{1L} \times Q_{\text{inv}}^{1L} + \mu_{1T} \times Q_{\text{inv}}^{1T} + \mu_{2L} \times Q_{\text{inv}}^{2L} + \ldots \right) \]

n-MOSFET energy band diagram

From F. Prégaldiny, PhD

A. Emrani, PhD INP Grenoble (1992)
1 - MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

⇒ LF noise: physical mechanisms

Normalized drain current power spectral density $\frac{W_{LSld}}{I_d^2}$

1\textsuperscript{st} term: Standard McWhorter carrier number fluctuations ($\Delta N$)

Ghibaudo model:

$$S_{I_d} = \left[1 + \alpha \mu C_{ox} \frac{I_d}{G_m}\right]^2 G_m^2 S_{Vfb}(f) \quad [A^2/Hz]$$

2\textsuperscript{nd} term: Correlated mobility fluctuations ($\Delta \mu$) at high current
Matching of MOS transistors

MC analysis with ELDO after EKV parameter extraction

\[
\frac{\sigma(\Delta I_d)}{I_d} = \frac{1}{n U_t} \sigma(\Delta V_{T0})
\]  
(Eq. 1)

- Fair agreement between measurements and MC simulations (for relative mismatch higher than ~ 0.5%)
- Higher current mismatch at low temperature
MOSFET compact modeling for design of mixed A/D circuits at cryogenic temperature

| Design of high performance hybrid infrared CMOS image sensors working at low temperature |
| Bispectral IR imager from CEA-Leti |

- Format=256 x 256, pitch=30 μm
- Complex CMOS circuit, approx. number of transistors: 530,000
- 0.35 μm / 3.3 V CMOS process
- Full parameter extraction at intermediate temperature (77 - 200 K):
  - DC, AC, LF noise, matching and temperature parameters
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AlGaN/GaN HEMT schematic structure

Lattice constants:

- $a_{\text{Si}} = 0.54 \text{ nm}$
- $a_{\text{GaN}} = 0.32/0.51 \text{ nm}$ (a/c axis)

Important $\Delta a/a$

Thermal conductivity:

- $K_{\text{Si}} = 150 \text{ W/m.K}$
- $K_{\text{GaN}} = 130$
- $K_{\text{SiC}} = 320$
Leti-HSP model flow

- Parameters
  - Polarization effects (SP, PZ)
  - Temperature modeling
    - Incomplete donor ioniz.
    - DIBL Effect
- Electrostatics
  - $\Phi_{ss}$, $\Phi_{sd}$, $\Phi$, $\Phi_{sm}$
- Mobility
- Velocity Saturation
- Channel Length Mod.
- $V_{off}$
- Drain current (Ids)
  - Access resistances
  - Self-heating
- 2DEG charge ($Q_i$)
  - Charge partitioning ($Q_s/Q_d$)
  - Parasitic cap.
- Schottky gate current (Ig)

VBA and Matlab code development
Verilog-A code implementation
Parameter extraction + literature data
Circuit simulation using ADS (Keysight Tech.)

Leti-HSP, a Surface-Potential-Based Compact Model of AlGaN/GaN HEMTs Power Transistors
Results: DC current and self-heating

Verilog-A code + ADS simulation

L=1 µm and W=75 µm
Compact Modeling Coalition (CMC): Selection of a power GaN HEMT model

- Process for standardization in 4 phases
- 10 models selected during phase 1
- 4 models still in phase 2:
  - ASM: University of California, Berkeley, USA
  - MVSG: Massachusetts Institute of Technology, USA
  - Angelov: Chalmers University, Sweden
  - HSP: CEA-Leti, France
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Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

CMOS Process Design Kit (PDK) and ASICs design flow

Resistor, diode, transistor, etc. but no waveguide, no photodetector, no laser diode, no light modulator, etc.
3 - Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

Photonics PDK and Application Specific Photonics ICs (ASPICs) design flow

- Waveguide, photodetector, laser diode, light modulator, etc.
Photonics device modeling

To simulate a device we need:

- The optical/electro-optical model (optical losses, phase shift, electro-optical effect): coded in Verilog-A

- The optical and electrical I/O: optical I/O are described by an optical bus of 9 lines

- The electrical model (R-L-C-G from electrical contacts, extrinsic elements due to BOX and HR substrate in the Leti SOI photonics process, etc.): described by a macro-circuit inside a SPICE netlist
### Photonics device modeling

**Popt**: optical power, **pol**: light polarization, **Φ**: optical phase

**Driving circuitry**

- **Popt**₀(\(f_{\text{opt}}, \text{pol}, \phi\))
- **CW laser**

**Passive device** (e.g. WG)
- \(\Phi_{\text{opt}}(f_{\text{opt}}, \text{pol}, \phi)\)

**MZI modulator** (bias)
- \(G_{\text{E/O}}(f_{\text{elec}}, f_{\text{opt}}, \text{pol})\)

**Photo-Detector** (bias)
- \(G_{\text{O/E}}(P_{\text{opt}}, f_{\text{opt}}, f_{\text{elec}}, \text{pol})\)

**Passive device** (e.g. WG)
- \(G_{\text{passive}}(f_{\text{opt}}, \text{pol}, \phi)\)

**Reading circuitry** (e.g. TIA)
- \(i(t)\)

**Output**
- \(u_{\text{out}}(t) = Z \times i(t)\)

\[P_{\text{opt}}_1 = G_{\text{E/O}}(f_{\text{elec}}, f_{\text{opt}}, \text{pol}) \times u_{\text{in}}(t) \times P_{\text{opt}}_0(f_{\text{opt}}, \text{pol}, \phi)\]

\[P_{\text{opt}}_2 = G_{\text{passive}}(f_{\text{opt}}, \text{pol}, \phi) \times G_{\text{E/O}}(f_{\text{elec}}, f_{\text{opt}}, \text{pol}) \times u_{\text{in}}(t) \times P_{\text{opt}}_0(f_{\text{opt}}, \text{pol}, \phi)\]

\[i(t) = G_{\text{O/E}}(P_{\text{opt}}, f_{\text{opt}}, f_{\text{elec}}, \text{pol}) \times G_{\text{passive}}(f_{\text{opt}}, \text{pol}, \phi) \times G_{\text{E/O}}(f_{\text{elec}}, f_{\text{opt}}, \text{pol}) \times u_{\text{in}}(t) \times P_{\text{opt}}_0(f_{\text{opt}}, \text{pol}, \phi)\]
3 - Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

Optical bus

The optical signal is represented by 9 variables:
• one variable is the wavelength $\lambda$
• $2 \times 2 \times 2 = 8$ other variables to describe the optical field

2 possible directions 2 possible polarizations

Real part and imaginary part (in $W^{1/2}$)

The wavelength is the same for every devices connected together. It's the central wavelength of the simulation, usually chosen as the laser wavelength

• $A_x$ and $A_y$ are the complex amplitude of the two polarization modes
• Complex amplitude more practical than power & phase (linear equations, no discontinuity, less equations)
3 - Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

Influence of SOI process integration (MIEL conf. 2014)

Macro-model: \( R, L, C = f (L_{\text{arm}}, L_{\text{junction}}, T_{\text{box}}, T_{\text{Si}}, \text{etc.}) \)

\( R, L = f (\text{Frequency}) \)
3 - Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

SPICE toolbox of passive and active silicon photonics devices / Symbols
Example: Building an optical link like a Lego® game

Optical Source (OS)

Waveguide (WG)

Photodiode (PD)
3 - Verilog-A models for silicon photonics devices and implementation in a standard EDA environment

Example: TRAN simulation of an optical link (ADS simulator from Keysight, Eldo simulator from Mentor Graphics)
Example: Variability study in a purely passive optical device, such as a waveguide, with an electrical simulator (Eldo, Mentor Graphics)

Monte Carlo analysis / Number of runs=1000
Optical input power=1.000 W / λ=1.55 µm / T=25 °C / WG_LENGTH=1m DEV/GAUSS=10 %

Database : test_WG9 leftist MC

m=0.955 W
σ=4.4 mW (0.46%)

SOI WG, propagation loss: 2 dB/cm
SPICE compact modeling is sometimes a very difficult task due to physics (and mathematics!)

but

is a prerequisite to design innovative ICs
Some references

Reference on cryogenic CMOS:

http://www.mos-ak.org/rome/talks/T04_Martin_MOS_AK_Rome.pdf

References on power transistors:


References on silicon photonics:


Thank you for your attention

ध्यान देने के लिए आपका धन्यवाद