Several Issues for Analog Design with a 0.18 µm CMOS Technology at Low Temperature

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1. Abstract

A detailed temperature analysis between 77 K and room temperature of several physical effects in a dual voltage CMOS technology with 0.18 µm / 1.8 V and 0.35 µm / 3.3 V MOSFET transistors is performed. These effects must be accurately accounted for in compact models used for simulation of analog circuits working at low temperature. Sub-bands quantum mechanical effects, Gate Induced Drain Leakage (GIDL) and Drain Induced Threshold voltage Shift (DITS) are investigated in this paper.

2. Introduction

This paper deals with the simulation of hybrid CMOS readout circuits working at low or at intermediate temperature, typically 77 K, 130 K or 200 K, such as those used in high performance infrared image sensors [1, 2]. These high complexity sensors have typically 1000 x 1000 pixels with a pitch of 15 µm and several transistors per pixel. The most critical electronic part is the analog block which interfaces with the photoelectric diode sensitive to infrared radiations. The photocurrent delivered by this diode is extremely low, typically some nanoamperes, and the MOSFET transistors are operating in the weak inversion regime for direct-injection read-out circuits. Digital blocks are also used to process the signals, inside or outside the pixel. SPICE parameters of transistors, including DC, AC, 1/f noise and matching parameters, are mandatory for precise simulation and optimization of such mixed circuits. So, the MOSFET compact model used during electrical simulations must be very precise and must include physical effects. We have previously reported different effects, specific or not, to low temperature operation [3, 4]. In this paper, other physical phenomena which are important for analog modeling are studied in a 0.18 µm CMOS technology.

3. CMOS process

We characterize a commercial mixed mode / RFCMOS process optimized for room temperature operation. In this dual gate oxide process, two kinds of MOSFET transistors are available: (1) transistors with a physical gate oxide thickness of 3.3 nm, a minimum channel length of 0.18 µm and operating at a maximum recommended voltage of 1.8 V and (2) transistors with a physical gate oxide thickness of 6.5 nm, a minimum channel length of 0.35 µm and operating at 3.3 V. p-MOSFET are made in a NWELL. Depending on the channel doping, transistors with different threshold voltages are provided. p-MOSFET transistors may be done either with a standard threshold voltage (STD) or with a low threshold voltage (LVT). n-MOSFET transistors are made either in a P-substrate (also referred as the PWELL) or in a triple well (TWELL). N-MOSFET transistors have either a standard threshold voltage (STD), a low threshold voltage (LVT) or a zero-volt threshold voltage (ZVT). As a whole, twelve MOS transistors are allowed for mixed analog-digital circuit design. This deep submicron process has pocket implants to control short channel effects. Finally we have to mention that this process has LDD zones to diminish hot-carrier degradation and use Shallow-Trench Isolation (STI).

4. Subband quantum effects

In some transistors of the process, namely 1.8 V LVT NMOS transistors, we observed a peak in the gate transconductance characteristics, Gm vs. Vgs, at low temperature (Fig. 1). This peak is observed in moderate inversion, at the beginning of strong inversion. Such a peak has been already observed at intermediate temperature (77 - 120 K) on some CMOS processes [5].

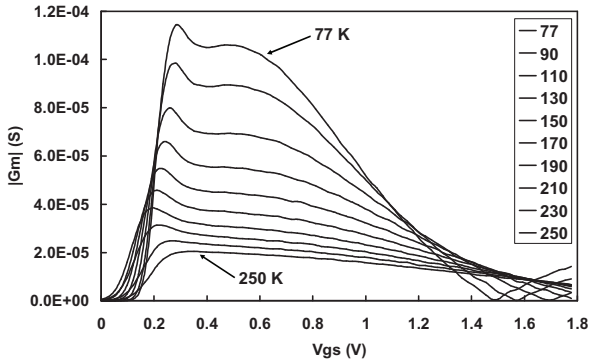

Fig.1. *Absolute value of the gate transconductance Gm measured at different temperatures for 1.8 V LVT NMOSFET with W/L=13/13, Vds = 50 mV, Vbs = 0 V (note that Gm becomes negative for high Vgs at low temperature).*

We have shown [4, 6] that this peak could be interpreted as the result of energy quantization in the inversion layer. Energy subband separation effect is enhanced at very low temperature or at very high effective transverse field E_{eff} at the Si/SiO_2 interface given by eq. 1:

$$E_{eff} = \frac{\eta\, Qi + Qb}{\varepsilon_{Si}}, \qquad (1)$$

where η = 1/2 for NMOS and 1/3 for PMOS, Qi is the inversion charge and Qb the depletion charge.

At not too low temperature, different subbands with different mobility are filled. The occupancy of these subbands is modified by E_{eff}. As E_{eff} is proportional not only to the inversion charge Qi but also to the depletion charge Qb, subbands occupancy can also be varied by the channel doping Nch or by the bulk voltage Vbs as Qb is given by eq. 2:

$$Qb = \sqrt{2\, q\, \varepsilon_{Si}\, Nch\, (\psi_s + Vsb)}. \qquad (2)$$

In order to observe the peak in the Gm vs. Vgs characteristic, the first excited subband must be filled. So the temperature must not be too low, otherwise only the fundamental subband will be filled. The effective transverse electric field must also be low enough. This last condition is achieved for low Vgs (low Qi), and/or low Nch or low Vbs (low Qb). This interpretation is consistent with the fact that we observe this phenomenon only on low doped transistors, i.e. on LVT transistors, and not on STD transistors where the channel doping is higher. It is also coherent with the fact that we observe it only on long channels and not on transistors shorter than 2 µm. As a matter of fact, due to the Reverse Short Channel Effect (RSCE) existing in these transistors, the effective channel doping increases as the channel length decreases and the Gm peak is no more observed.

Fig. 2 shows the evolution of the Gm peak, normalized to its value estimated at Vgs = 0.4 V, as a function of temperature for a long channel 1.8 V LVT NMOSFET (L = 13 µm). This peak first increases up to a temperature of 180 ~ 200 K, and then decreases. This quantum mechanical effect is not accounted for in any advanced MOSFET compact models, such as EKV3, PSP or HiSIM, which were developed for temperatures around the ambient.

Fig. 1 shows also that the gate transconductance Gm measured in the ohmic mode (Vds = 50 mV) could be negative on cooled NMOS transistors at high vertical fields. The explanation is that, when increasing Vgs, the increase of the inversion charge cannot compensate for the high mobility attenuation. The drain current will decrease, so Gm becomes negative.

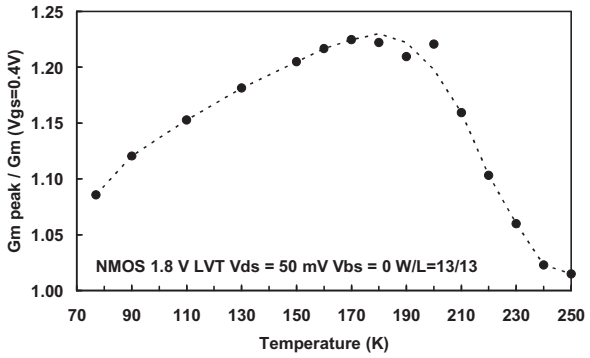

Fig.2. *Evolution of the Gm peak / Gm (Vgs = 0.4 V) ratio as a function of temperature (1.8 V LVT NMOSFET).*

5. Gate Induced Drain Leakage at low temperature

Gate induced drain leakage (GIDL) could constitute an important issue as regard to the off-state current in MOS devices used in infrared or visible CMOS imagers during integration of extremely low currents. GIDL current is attributed to band-to-band tunneling taking place in the deep-depleted region underneath the gate oxide, when the gate is grounded and the drain is biased at high voltage. Some devices of the studied process exhibit a noticeable GIDL current. For example, results on GIDL current in 3.3 V STD PMOSFETs at three temperatures are shown in Fig. 3.

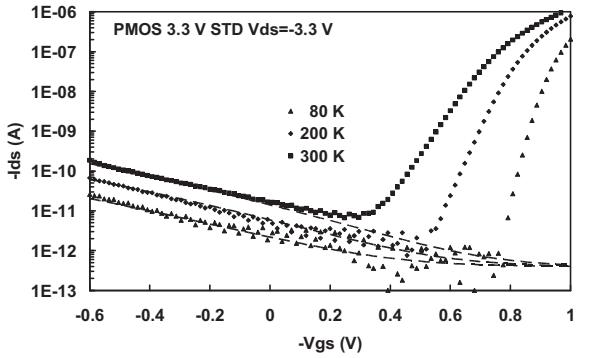

Fig.3. *Typical transfer characteristics illustrating the GIDL current at three temperatures. Experimental (symbols) and calculated (dashed lines) curves using eq. (3).*

The GIDL current is measured as a function of gate voltage for a fixed drain bias (Vds = -3.3 V) for a device with channel width W = 20 µm and channel length L = 20 µm. The noise floor level is around 0.5 pA and is due to electrical wiring inside the cryostat. In contrast to common expectation for a tunneling process, the GIDL current is actually found to decrease substantially with temperature.

In order to calculate the contribution of this effect to the drain current, we use the classical GIDL model [7]:

$$Ids = W\ A_{GIDL}\ E_S\ exp\left(-B_{GIDL}/E_S\right) \quad (3)$$

$$with\ E_S = \frac{\left(Vds - Vgs - E_{GIDL}\right)}{3\ Tox}, \quad (4)$$

where A_{GIDL}, B_{GIDL} and E_{GIDL} are coefficients. The oxide thickness Tox of 3.3 V MOSFETs is 6.5 nm.

Fig. 4 shows that the extracted B_{GIDL} coefficient is found to be nearly constant with temperature using E_{GIDL} = 1.2 V. The mean value is 4.5 x 10^9 V/m or 45 MV/cm and is close to the theoretical value (30 - 40 MV/cm). However, the A_{GIDL} coefficient is temperature dependent and decreases by almost one order of magnitude between room temperature and liquid nitrogen temperature. This change is much more important that the 7 % expected variation between these temperatures, due to the silicon energy gap Eg(T) evolution, as A_{GIDL} is proportional to Eg^2. This behavior was first reported by Rais [8]. Then Ghibaudo and Balestra [9] have suggested that a better modeling of the band-to-band tunneling process is needed at low temperature.

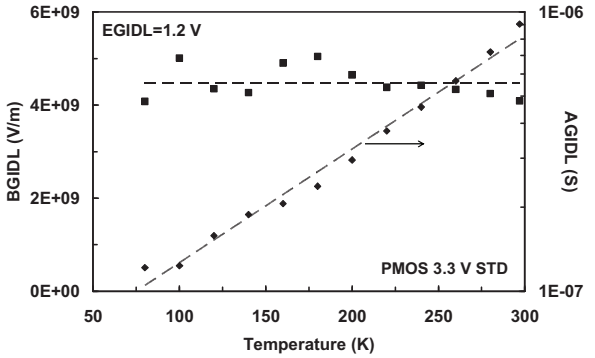

Fig.4. *Variation of the GIDL coefficients A_{GIDL} and B_{GIDL} with temperature.*

6. Drain Induced Threshold voltage Shift at low temperature

Pocket implants are widely used in 0.18 µm technology node, and beyond, to control short channel effects and to reduce threshold voltage (Vth) roll-off and also punch-through [10]. This technique, however, produces large Drain-Induced Threshold voltage Shift (DITS) and increases the output conductance Gds in long channel devices [11]. This effect may greatly affect analog circuit performance, especially when transistors are working in weak inversion.

The difference between the saturated threshold voltage (Vth Sat) and the linear threshold voltage (Vth Lin) versus gate length for 1.8 V and 3.3 V NMOS devices was measured at 295 K and 77 K. Vth Lin was measured at Vds = 50 mV using the constant current method. This method introduces no artifact when carrier freeze-out effects occur at low temperature in 3.3 V devices, in contrast to the linearly extrapolated method which is the most common method of measuring Vth [12]. Vth Sat was measured at Vds = 1.8 V or 3.3 V, using also the constant current method. Fig. 5 shows that, as expected, 3.3 V devices having no pockets exhibit a lower DITS effect than 1.8 V devices having pockets. The threshold voltage shift is 60 % larger for the pocket implanted device at long gate lengths at room temperature and 5 times larger at 77 K.

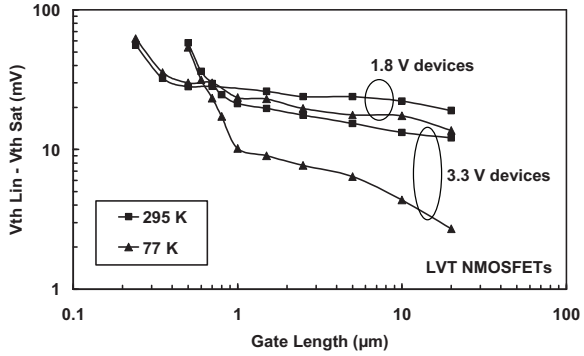

Fig.5. *DITS in 1.8 V (with pockets) and 3.3 V (w/o pockets) NMOSFETs at 295 K and 77 K.*

The first physical model of DITS suitable for compact modeling was reported by Cao et al. [13] and verified against experimental data from a 0.18 µm CMOS technology at room temperature. They have shown that the threshold voltage shift due to this effect is given by:

$$\Delta Vth_{DITS} = -S\ log\left(\frac{\left(1 - exp\left(-\beta\ Vds\right)\right)}{1 + \left(1 + exp\left(-C_2\ Vds\right)\right)/C_1\ L}\right), \quad (5)$$

where $\beta = q/kT$, S the subthreshold swing and C_1 and C_2 are the two fitting parameters of the model.

Fig. 6 shows the best experimental data fitting obtained by this model after optimization of C_1 coefficient at each temperature.

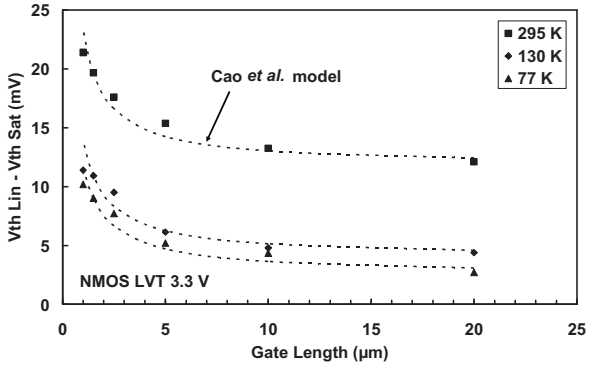

Fig.6. *Fitting of DITS experimental data with the Cao et al. model for 3.3 V LVT NMOSFETs.*

Actually, C_1 coefficient is found to be not constant, but varying with temperature as shown in Fig. 7. Equation (5) could then be used for DITS modeling at any temperature between 77 K and room temperature provided a linear dependency of the C_1 parameter with temperature is used.

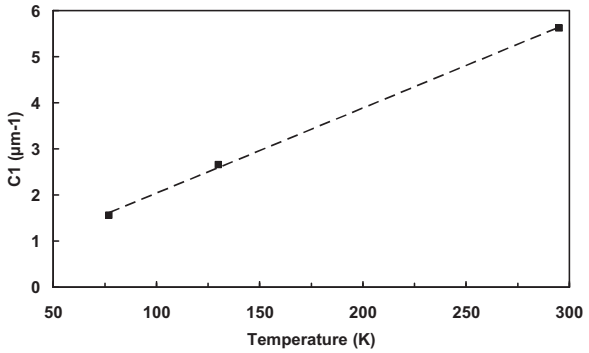

Fig.7. *Evolution with temperature of the DITS coefficient C_1 in 3.3 V LVT NMOSFETs.*

7. Conclusion

We have presented experimental data on several physical effects in a dual gate oxide CMOS technology between 77 K and 300 K. These effects, and also their temperature dependencies, must be accurately modeled for simulation of analog circuits working at low temperature. Sub-bands quantum mechanical effects, gate induced drain leakage and drain induced threshold voltage shift were investigated in this paper. In order to obtain an accurate low temperature modeling, a temperature dependence of relevant parameters has successfully been introduced in compact models of the MOS transistor.

Acknowledgments

The authors would like to acknowledge helpful discussions with Marina Reyboz and colleagues from the imagers design team in LETI. This work was sponsored by DGA (Délégation Générale à l'Armement), Ministry of Defense, France.

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