MOS Transistor Matching at Low Temperature for Analog Circuit Design

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1. Abstract

MOSFET matching parameters are measured at low temperature (77 - 130 K) for simulation of mixed analog-digital circuits used in cooled infrared image sensors. This study is performed on a dual gate oxide CMOS technology with 0.18 µm / 1.8 V and 0.35 µm / 3.3 V MOSFET transistors. Freeze-out effects in Lightly Doped Drain (LDD) regions are observed at low temperature and their impact on threshold voltage measurements is detailed. Matching data at different temperature are presented. A good agreement between experiments and Monte-Carlo simulations with the EKV2.6 compact model of the MOS transistor is observed.

2. Introduction

This paper deals with the simulation of hybrid CMOS read-out circuits working at low or at intermediate temperature, typically 77 K, 130 K or 200 K, such as those used in high performance infrared image sensors [1]. SPICE parameters of transistors, including DC, AC, 1/f noise and matching parameters, are mandatory for design and simulation of such circuits. However, as CMOS manufacturers do not provide full sets of MOSFET parameters for simulation at temperature lower than -55°C (≈ 220 K), these parameters must be extracted prior to circuit simulation. Furthermore the used MOSFET compact model must address the important weak and moderate inversion regimes where most of the analog transistors of the CMOS read-out circuits are operating. Matching characterization is an essential aspect in such analog circuits as it allows taking into account the electrical differences that occur between identically designed transistors of different gate area. The mismatch model proposed in 1989 by Pelgrom [2] is widely used to predict theses differences and states that the standard deviation in the mismatch of electrical parameter P between two identical MOS transistors of width W and length L separated by a distance D is given by:

$$\sigma^2(\Delta P) = \frac{A_P^2}{W\,L} + S_P^2\,D^2\,, \qquad (1)$$

where A_P and S_P are area and spacing parameter, respectively. In this work we report experimental data at low temperature on transistor matching and methodology of parameter extraction for a commercial CMOS process.

3. CMOS process

We characterize a mixed mode process optimized for room temperature operation. In this dual gate oxides process, two kinds of MOSFET transistors are available: (1) transistors with a physical gate oxide thickness of 3.3 nm, a minimum channel length of 0.18 µm and operating at a maximum recommended voltage of 1.8 V and (2) transistors with a physical gate oxide thickness of 6.5 nm, a minimum channel length of 0.35 µm and operating at 3.3 V. P-MOSFET are made in a NWELL. Depending on the channel doping, transistors with different threshold voltages are provided. P-MOSFET transistors may be done either with a standard threshold voltage (STD) or with a low threshold voltage (LVT). N-MOSFET transistors are made either in a P-substrate (also referred as the PWELL) or in a triple well (TWELL). N-MOSFET transistors have either a standard threshold voltage (STD), a low threshold voltage (LVT). As a whole, twelve MOSFET transistors are allowed for mixed analog-digital circuit design. This process uses two kinds of polysilicon gates, N^+ doped polysilicon gate for N-MOSFET and P^+ doped polysilicon gate for P-MOSFET. This deep submicron process has pocket implants to control short channel effects. Finally we have to mention that this process use Shallow-Trench Isolation (STI) and has LDD zones to diminish hot-carrier degradation and we will see their impact at low temperature.

4. Extraction of the threshold voltage at low temperature

Prior to parameter extraction using a compact model, a fine characterization of the different transistors at various temperatures is performed. This step is mandatory to examine different effects, namely we will focus on the carrier freeze-out effect in the LDD regions observed on 3.3 V NMOS transistors of this technology when the temperature is lower than 150 K [3]. This phenomenon leads to an important decrease of the drain conductance Gds at low drain-to-source voltages (less than 250 mV) in strong inversion when the impact of series resistances is not negligible (see Fig. 1).

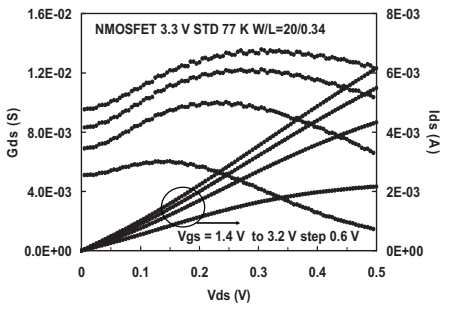

***Fig 1**. Carrier freeze-out effect in LDD regions for 3.3 V STD NMOSFET at 77 K.*

Numerous methods exist in order to extract the threshold voltage, VT0 [4]. Most of them are based on measurements of drain current Ids for various values of

gate voltage Vgs, at low Vds (typically 50 mV) to ensure operation in the linear region. We have tested four methods and discuss their applicability at low temperature.

1 - Extrapolation method. In this method, VT0 is defined as the gate voltage which is obtained by extrapolating the linear portion of the Ids (Vgs) characteristics, from the maximum slope, to zero drain current. We use this method to characterize the reverse short channel effect (RSCE) observed with this technology. The threshold voltage shift, defined as $\Delta VT0 = VT0 - VT0 (L = 20\ \mu m)$, is plotted in Fig. 2 as a function of the gate length for 3.3 V NMOSFET. Using this extrapolation method, we would conclude that the expected RSCE effect is absent at low temperature and that an anomalous short channel effect is observed.

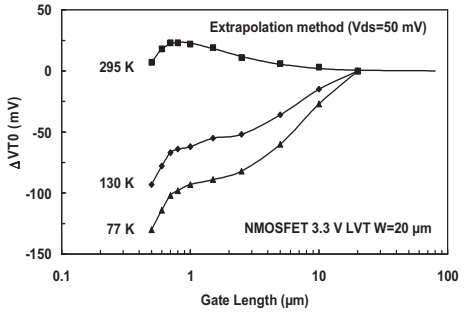

***Fig. 2**. Characterization of the RSCE effect at different temperatures using the extrapolation method.*

2 - Constant current method. In this method, the gate voltage Vgs at a specific drain current Ids is taken to be the threshold voltage. We choose a specific value of 100 nA and verify that almost the same behavior is obtained with values of 10 nA and 1 µA. Fig. 3 shows that, by using this method, the RSCE effect is still observed at low temperature and that no anomaly occurs.

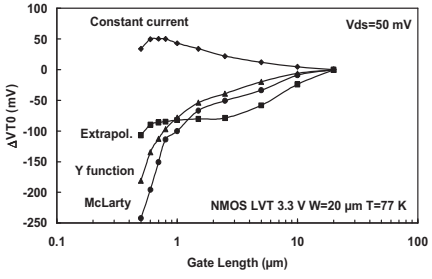

***Fig. 3**. Threshold voltage shift at 77 K using different extraction methods.*

3 - Y function method [5]. One may think that, due to the freeze-out effect occurring at low temperature, the LDD zones are highly resistive and perturbed the VT0 extraction at high Vgs. The Y function method ($Y = Ids/\sqrt{Gm}$), proposed by Ghibaudo, is supposed to alleviate from these problems, at least at room temperature. As for the extrapolation method, Fig. 3 shows that, by using this method, we would also conclude that the RSCE effect is no more observed at low temperature.

4 - McLarty method [6]. This method was developed for ultra thin oxides. Fig. 3 shows that, by using this method, we would also conclude that the RSCE effect is not observed at low temperature.

In conclusion, when carrier freeze-out in LDD regions at low temperature is effective, the constant current method is the only method which is applicable for VT0 extraction as it does not lead to SCE artifacts. This is the only method where VT0 extraction is conducted in weak inversion and is thus the less sensitive method to series resistance effects.

5. Matching test structures and experimental procedure

To investigate the matching properties of this 0.18 / 0.35 µm CMOS process, several modules of NMOS and PMOS transistors with different W/L ratios have been measured. Each module contains 21 transistors of the same size drawn along a line and separated by 15 µm. This leads to 210 transistor pairs. A summary of the LVT device geometries is given in the following table.

***Table I**. Matching test structures for LVT transistors*

Transistors	W (µm)	L (µm)	Area (µm²)
NMOS and PMOS 1.8 V	13	13	169
Tox = 3.3 nm	0.9	0.9	0.81
	0.5	0.5	0.25
	0.44	0.24	0.106
NMOS and PMOS 3.3 V	13	13	169
Tox = 6.5 nm	1.3	1.3	1.69
	0.7	0.7	0.49
	0.44	0.5	0.22

All devices are measured at low temperature and matching parameters of the Pelgrom model are extracted at 77 K, 130 K and 295 K. All dies are mounted inside a cryostat. A switch matrix allows automatic measurements while it is driving by the UTMOST software from SILVACO. This software is also used to extract the three parameters useful for matching study:

1. The threshold voltage VT0 and the current factor β ($= \mu C_{ox}$) are extracted from Ids (Vgs) measurements in the linear regime (Vds = 50 mV) at Vbs = 0 V.
2. The body effect parameter γ is extracted from Ids (Vgs) measurements at different bulk voltages.

6. Results on Transistor matching

A. Measurements of distance parameters S_P

The Pelgrom equation given above suggests that, for transistors of large area, the size dependent contribution

vanish and that the distance term $S_P^2 D$ could be evaluated, allowing extraction of the S_P parameters. Fig. 4 shows the dispersion of the parameter VT0 as a function of the distance D between two transistors at 77 K. The slope of this plot gives the S_{VT0} parameter.

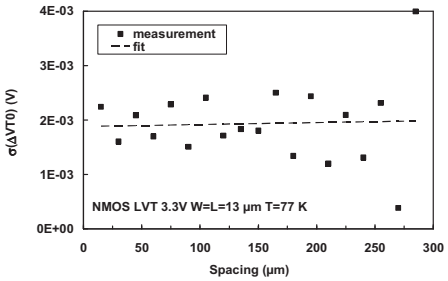

***Fig. 4**. VT0 dispersion of NMOS LVT 3.3 V versus the spacing between transistors at 77 K for W=L=13 µm.*

Distance parameters S_{VT0}, S_β and S_γ measured for NMOS LVT 3.3 V at different temperatures are listed in table II.

***Table II.** Matching parameters depending on distance for NMOS 3.3 V LVT*

Parameter	Units	295 K	130 K	77 K
S_{VT0}	µV/µm	0	0	0.4
S_β	%/µm	0	$1.3\ 10^{-3}$	$2.7\ 10^{-4}$
S_γ	$V^{1/2}$/µm	$1.8\ 10^{-7}$	$1.4\ 10^{-6}$	$3.8\ 10^{-6}$

We have verified that the S_P terms are so low that we can neglect them and consider only the A_P terms. This observation is also verified for other transistors: PMOS LVT 3.3 V and NMOS-PMOS LVT 1.8 V.

B. Measurements of area parameters A_P

Matching parameters at different temperatures for the threshold voltage VT0, current factor β and substrate factor γ using equation (1) were measured on 1.8 V and 3.3 V LVT transistors. To illustrate these measurements, Fig. 5 presents the extraction of the A_{VT0} and A_β matching parameters for PMOS LVT 3.3 V at 77 K.

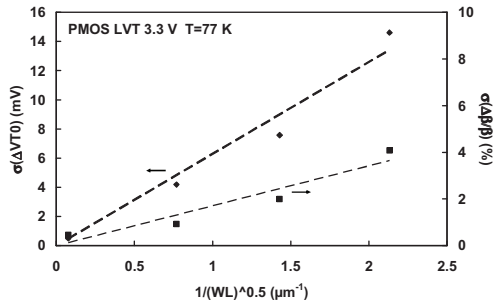

***Fig. 5**. Extraction of Pelgrom parameters A_{VT0} and A_β from dispersion measurements at 77 K.*

Evolution with temperature of the matching parameters of different devices is shown in Fig. 6, 7 and 8. These parameters are not constant in the temperature range 77 K - 300 K. A_β and A_γ parameters systematically increase at low temperature for the different transistors. Concerning the A_{VT0} parameter, it is either constant or increases at low temperature, depending on the type of transistor. Such a behavior was already observed on a different CMOS technology [7]. The A_{VT0} / T_{ox} ratio of this process at 77 K is typically 2.1 ~ 2.2 mV.µm / nm, except for 3.3 V PMOS where it is ~ 1 mV.µm / nm. It should be noted that an increase of A_{VT0} parameter at low temperature is theoretically expected from the enlargement of the depletion layer at low temperature, since the number of dopants in the depletion zone is increased.

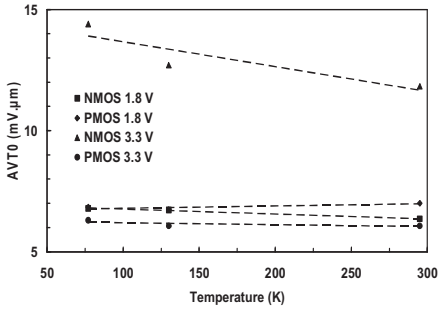

***Fig. 6**. Evolution with temperature of the A_{VT0} parameter.*

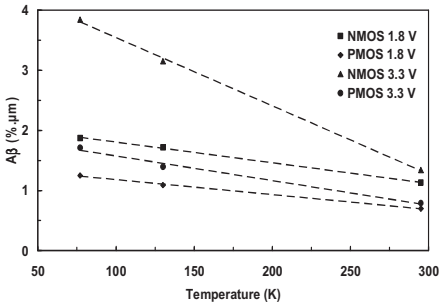

***Fig. 7**. Evolution with temperature of the $A\beta$ parameter.*

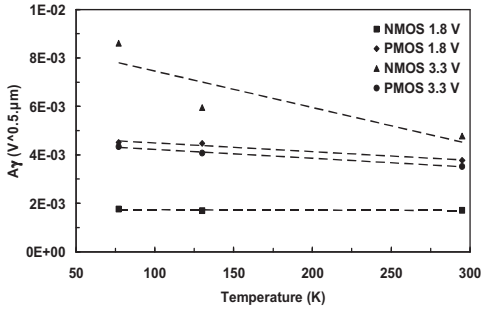

***Fig. 8**. Evolution with temperature of the $A\gamma$ parameter.*

7. Monte-Carlo simulations

Extracted matching parameters were then used during Monte-Carlo (MC) simulations of the drain current difference $\Delta Id = Id_1 - Id_2$ and its fluctuation $\sigma(\Delta Id)$ between identically drawn transistors biased at the same Vgs. In this work we use the standard version of the EKV 2.6 compact model [8] because it is known to be valid and continuous in all operating regions of the MOSFET, from weak to strong inversion and from

triode to saturation. EKV2.6 model parameters were previously extracted on different devices at different temperatures. These Monte-Carlo simulations, performed with the Eldo electrical simulator from Mentor Graphics, are shown in Fig. 9 and 10, along with experimental data. The MOS transistors, PMOS LVT 3.3 V in this case, were biased in saturation (|Vds| = 3.3 V) at Vbs = 0 V. A satisfactory agreement between simulations and measurements is observed in the weak, moderate and strong inversion regimes, at room and low temperature. The relative drain current fluctuation is given by:

$$\frac{\sigma^2(\Delta Id)}{Id^2} = \left(\frac{Gm}{Id}\right)^2 \sigma^2(\Delta VT0) + \frac{\sigma^2(\Delta\beta)}{\beta^2}. \qquad (2)$$

Fig. 9 and 10 show also the calculated current fluctuation using only the ΔVT0 term. This is the predominant contribution in weak and moderate inversion. In weak inversion, the Gm/Id ratio is constant and the drain current mismatch is readily calculated by:

$$\frac{\sigma(\Delta Id)}{Id} = \frac{1}{n\,Ut}\,\sigma(\Delta VT0), \qquad (3)$$

where Ut is the thermal voltage (kT/q) and n the slope factor (n ~ 1.2-1.3 for 3.3 V PMOSFET).

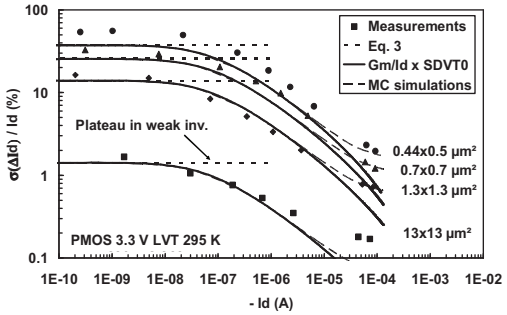

***Fig. 9**. Measured and Monte-Carlo simulated drain current mismatch in saturation (Vds=-3.3 V) from weak to strong inversion for 3.3 V LVT PMOSFET at 295 K of different W x L area. The solid line is calculated using only VT0 fluctuation in eq. 2. The plateau in weak inversion (dotted line) is calculated using eq. 3.*

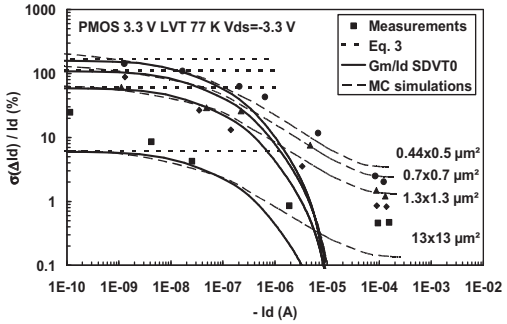

***Fig. 10.** Measured and Monte-Carlo simulated drain current mismatch at 77 K.*

8. Conclusion

We study MOSFET matching at room and low temperature on different transistors of a mixed 0.18 / 0.35 µm CMOS technology. We first discuss of different methods for the extraction of the threshold voltage. We find that, when freeze-out effects occur in LDD regions at low temperature, the constant current method is the most robust as it gets rid of high series resistance effects. No important variation of the mismatch with the spacing between transistors is experimentally found. The A_β and A_γ parameters increase at low temperature for the different devices. The A_{VT0} parameter is either constant or also increases at low temperature, depending on the type of transistor. These results have strong implications for design of cooled CMOS imagers. A fair agreement between measurements and Monte-Carlo simulations is observed from weak to strong inversion using the EKV model.

Acknowledgements

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