1/f Noise Modeling at Low Temperature with the EKV3 Compact Model

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ABSTRACT

We report on the characterization of Low-Frequency (LF) noise at room temperature and at low temperature (77 K) in a dual gate process with 1.8 V and 3.3 V MOSFETs. We found that the LF noise behavior in both n-MOSFETs and p-MOSFET of this process is well described physically by the correlated carrier number - mobility fluctuation model. We show that the flicker noise model introduced in the EKV3 compact MOSFET model allows to fit experimental data in a very wide range, from weak to strong inversion regimes.

Keywords: MOSFET, 1/f noise, low temperature, EKV3, compact model.

1 INTRODUCTION

This paper deals with the simulation of CMOS readout circuits working at low temperature (77 to 200 K), such as those used in high performance infrared image sensors [1]. SPICE parameters of transistors, including DC, AC, 1/f noise and matching parameters, are mandatory for design of such circuits. However CMOS foundries do not provide full sets of MOSFET parameters at low temperature. So these parameters must be extracted prior to circuit simulation. Furthermore, the used compact model must address the important weak and moderate inversion regimes where most of the analog transistors of the readout circuits are operating.

The EKV3 compact model was previously evaluated for simulation of mixed analog-digital circuits working at low temperature [2]. This evaluation was performed on a dual gate oxide CMOS technology with 0.18 µm / 1.8 V and 0.35 µm / 3.3 V MOSFET transistors. A detailed temperature analysis of some physical effects was performed. Specific effects, such as anomalous short and narrow channel effects or quantization of the inversion charge, were observed at low or intermediate temperature and we show that some improvements of this compact model will allow a very precise description of MOS transistors at low temperature.

This paper reports LF noise measurements of different MOSFETs at low temperature and its compact modeling. The CMOS technology is first presented. Thereafter, experimental setup is described. The third part is dedicated to the main results and 1/f noise modeling.

2 CMOS TECHNOLOGY

We characterize a mixed mode / RF CMOS process optimized for room temperature operation. In this dual gate oxide process, two kinds of MOSFET transistors are available: (1) transistors operating at a maximum recommended voltage of 1.8 V, having a physical gate thickness of 3.3 nm and a minimum drawn length of 0.18 µm and (2) transistors operating at 3.3 V, having a physical gate thickness of 6.5 nm and a minimum drawn length of 0.35 µm. p-MOSFET are made in a NWELL. Depending on the channel doping, transistors with different threshold voltages are provided. p-MOSFET transistors may be done either with a standard threshold voltage (STD) or with a low threshold voltage (LVT). n-MOSFET transistors are made either in a P-substrate (also referred as the PWELL) or in a triple well (TWELL). N-MOSFET transistors have either a standard threshold voltage (STD), a low threshold voltage (LVT) or a zero-volt threshold voltage (ZVT). As a whole, twelve MOSFET transistors are allowed for mixed analog-digital / RF circuit design. This process is a dual gate process and uses two kinds of polysilicon gates, N+ doped polysilicon gate for n-MOSFET and P+ doped polysilicon gate for p-MOSFET As a consequence both NMOS and PMOS are surface channel transistors. Low temperature characterization of this process was presented in [3].

3 LF NOISE MEASUREMENTS

LF noise was measured using a specific computer-controlled system with programmable biasing current amplifiers. This system allows automatic current fluctuations measurements. Low-noise voltage sources are used to bias drain, gate and bulk terminals. During noise measurements, transistors are biased in saturation (Vds = 1.8 or 3.3 V), and not as it is classically done in the linear regime (Vds ~ 50 mV), as it will be more representative of their operation in analog circuits [4]. Prior to noise measurements, the devices are characterized in the DC mode using an Agilent 4155 parameter analyzer. Important quantities, such as drain current (Id), gate transconductance (Gm), drain conductance (Gds) and bulk transconductance (Gmb) are measured. The high sensitivity of our experimental set-up allows to measure the thermal noise floor at frequency lower than 100 kHz on long channels biased in weak inversion. Different gate lengths have been under investigations from 20 µm to the minimum

allowed transistor length (0.18 or 0.35 µm), with gate widths from 20 µm to 1 µm. Transistors were biased at different gate voltages ranging from weak inversion (Id ~ 10 pA) to strong inversion (Id ~ 1 mA). The slope of each recorded spectrum is carefully analyzed. RTS noise components are eliminated. After this treatment, the LF noise is found to follow a $1/f^{\gamma}$ variation with a mean γ value of 1.0 ± 0.1.

4 RESULTS AND DISCUSSION

Several experiments were done in order to determine which one of the flicker noise models apply to these MOSFETs, McWhorter's carrier number or Hooge's mobility fluctuation model. Figures 1 and 2 show the experimental and simulated normalized drain current power spectral densities, SId/Id^2, on standard 3.3 V p-MOSFET, at 295 K and 77 K, respectively.

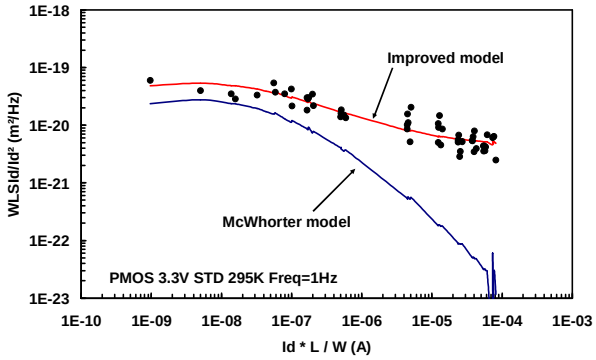

Figure 1: Experimental and best fit of WL x SId/Id^2 versus normalized drain current for 3.3 V STD p-MOSFET at 295 K.

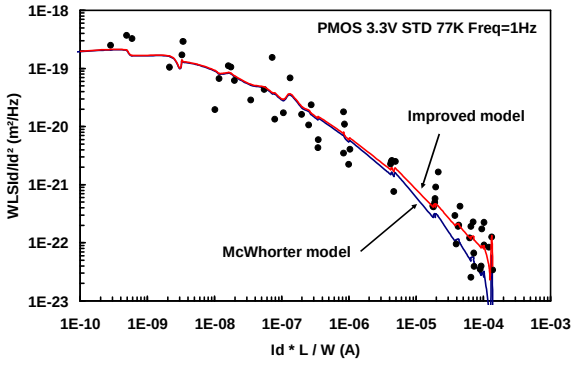

Figure 2: Experimental and best fit of WL x SId/Id^2 versus normalized drain current for 3.3 V STD p-MOSFET at 77 K.

The curves describe a plateau in weak inversion and agree well with the $(Gm/Id)^2$ characteristic. Experimental data were fitted using either the carrier number fluctuations model predicted by McWhorter, or the model improved by Ghibaudo et al. [5] by taking into account the correlated mobility fluctuations occurring at the highest currents:

$$SI_d = [1 + \alpha \mu C_{ox} \frac{I_d}{G_m}]^2 G_m^2 S_{Vfb}(f) \quad (1)$$

Where the flat-band voltage fluctuations are given by:

$$S_{Vfb}(f) = \frac{kT\, q^2\, \lambda\, N_t(E_F)}{WL\, C_{ox}^2} \frac{1}{f^{\gamma}} \quad (2)$$

$Nt\ (E_F)$ is the oxide trap volume density per unit energy ($eV^{-1}\ cm^{-3}$) evaluated at the Fermi level, λ a tunnel attenuation distance (0.1 nm) and α the Coulomb scattering coefficient (V s/C). Extracted values of α for 3.3 V STD p-MOSFETs are $3x10^5$ at 295 K and $5x10^3$ at 77 K.

Figures 3 and 4 show the experimental drain current power spectral densities SId versus Gm for 3.3 V STD PWELL n-MOSFET at 295 K and 77 K, respectively. Figures 5 and 6 show the same results for 3.3 V STD p-MOSFET.

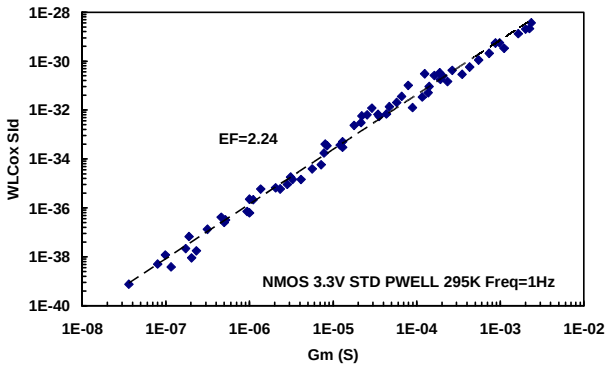

Figure 3: Experimental and best fit of WLCox SId versus Gm for 3.3 V STD PWELL n-MOSFET at 295 K.

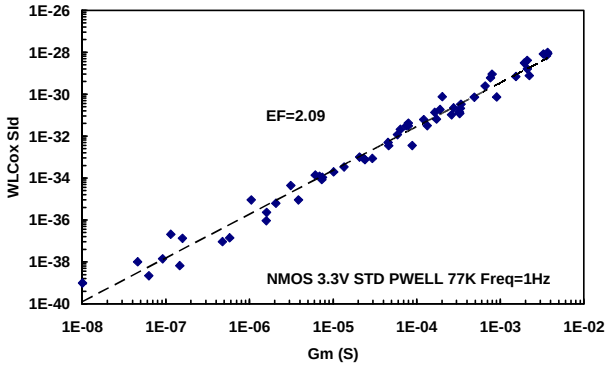

Figure 4: Experimental and best fit of WLCox SId versus Gm for 3.3 V STD PWELL n-MOSFET at 77 K.

NSTI-Nanotech 2009, www.nsti.org, ISBN 978-1-4398-1784-1 Vol. 3, 2009

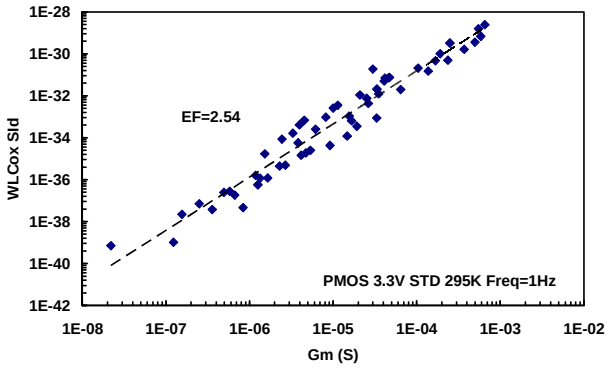

Figure 5: Experimental and best fit of WLCox x SId versus Gm for 3.3 V STD p-MOSFET at 295 K.

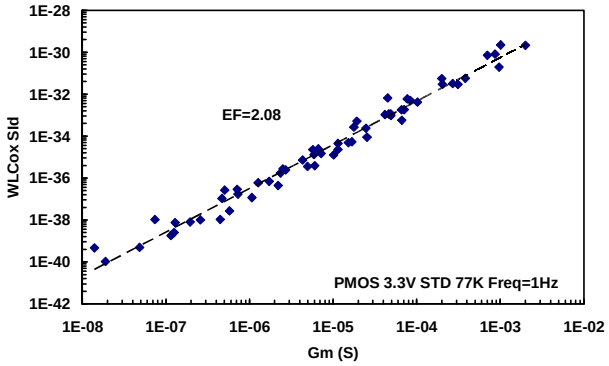

Figure 6: Experimental and best fit of WLCox x SId versus Gm for 3.3 V STD p-MOSFET at 77 K.

Figures 3-6 show that the following low-frequency noise model suits in a very large range of inversion for analog transistors used in the design of cooled or uncooled image sensors:

$$S_{Id} = \frac{KF\, G_m^{EF}}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \qquad (3)$$

where KF, EF and AF are parameters. This is the LF noise model introduced in the EKV3 charge-based compact model [6]. The extracted EF parameter is slightly different from 2, and lies between 1.7 and 2.4 on the different MOSFETs of this process. This result was previously reported on other advanced CMOS technologies [7].

5 CONCLUSION

In conclusion, experimental results on low frequency noise at room temperature and at 77 K for both NMOS and PMOS transistors have been presented. The 1/f noise behavior in both n-MOSFETs and p-MOSFET of this process is well described physically by the correlated carrier number - mobility fluctuation model. Typical values of the Coulomb scattering coefficient are about 10^4 V s/C for electrons and 10^5 V s/C for holes in silicon at room temperature. We observe that this parameter is temperature dependent and is lower at 77 K. The flicker noise model implemented in the EKV3 charge-based compact model was assessed in this work. This simplified 1/f noise model allows to fit experimental data, not only in the weak inversion regime, but also in the moderate and strong inversion regimes.

6 ACKNOWLEDGEMENTS

The authors would like to thank P. Maillart from Sofradir for design of test structures and M. Cavelier for technical assistance during DC and noise measurements. This work has been supported by DGA (Délégation Générale à l'Armement).

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