

EKV3 Compact Modeling of MOS transistors from a 0.18 μm CMOS Technology for Mixed Analog-Digital Circuit Design at Low Temperature

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EXTENDED ABSTRACT

This paper deals with the simulation of hybrid CMOS readout circuits working at low or at intermediate temperature, typically 77 K, 130 K or 200 K, such as those used in high performance infrared image sensors [1]. SPICE parameters of transistors, including DC, AC, 1/f noise and matching parameters, are mandatory for design and simulation of such circuits. However CMOS foundries do not provide full sets of MOSFET parameters for simulation at temperature lower than -55°C (220 K). So these MOSFET parameters must be extracted prior to circuit simulation. Furthermore the used MOSFET compact model must address the important weak and moderate inversion regimes where most of the analog transistors of the CMOS readout circuits are operating. A modified version of the EKV2.6 model [2] was previously described and was successfully applied to different CMOS bulk processes such as $0.7 \mu\text{m} / 5 \text{ V}$, $0.5\text{-}0.35 \mu\text{m} / 3.3 \text{ V}$ and $0.21 \mu\text{m} / 1.8 \text{ V}$ from different foundries at cryogenic temperature [3]. In this work we use the standard version of the EKV3 compact charge model [4]. The EKV3 model's performance is described in this paper for a commercial process, namely a dual gate oxide CMOS technology, with $0.18 \mu\text{m} / 1.8 \text{ V}$ and $0.35 \mu\text{m} / 3.3 \text{ V}$ MOSFET transistors.

We characterize a mixed mode/RFCMOS process optimized for room temperature operation. In this dual gate oxide process, two kinds of MOSFET transistors are available: (1) transistors with a physical gate thickness of 3.3 nm, a minimum channel length of $0.18 \mu\text{m}$ and operating at a maximum recommended voltage of 1.8 V and (2) transistors with a physical gate thickness of 6.5 nm, a minimum channel length of $0.35 \mu\text{m}$ and operating at 3.3 V. p-MOSFET are made in a NWELL. Depending on the channel doping, transistors with different threshold voltages are provided. p-MOSFET transistors may be done either with a standard threshold voltage (STD) or with a low threshold voltage (LVT). n-MOSFET transistors are made either in a P-substrate (also referred as the PWELL) or in a triple well (TWELL). N-MOSFET transistors have either a standard threshold voltage (STD), a low threshold voltage (LVT) or a zero-volt threshold voltage. As a whole, twelve MOSFET transistors are allowed for mixed analog-digital circuit design. This process is a dual gate process and uses two kinds of polysilicon gates, N^+ doped polysilicon gate for n-MOSFET and P^+ doped polysilicon gate for p-MOSFET. As a consequence both NMOS and PMOS are surface channel transistors and the threshold voltage temperature coefficients are nearly equal ($0.8\text{-}1.2 \text{ mV/K}$). This deep submicron process has pocket implants to combat short channel effects. Finally we have to mention that this process has LDD zones to diminish hot-carrier degradation and use Shallow-Trench Isolation (STI).

Prior to parameter extraction using a compact model, a fine characterization of the different transistors at different temperatures is needed. This step is mandatory to examine different effects, such as short channel and narrow width effects. We observed that NMOS and PMOS present a reverse short channel (RSCE) effect. The threshold voltage shift [$\text{DV}_{\text{th}} = \text{V}_{\text{th}} - \text{V}_{\text{th}}(L=20 \mu\text{m})$] is rather insensitive to the bulk voltage V_{bs} . Due to the RSCE effect, the V_{th} roll-up is observed. The V_{th} roll-off due to both charge sharing and Drain Induced Barrier Lowering (DIBL) is not observed. A significant reduction of this RSCE effect with temperature is observed. This reduction has been previously observed and interpreted as the variation of the threshold voltage with the Fermi bulk potential [5]. The RSCE effect is well modeled in the EKV2.6 and EKV3 compact models at a given temperature by using two parameters: LR and QLR. In order to obtain a very precise low temperature modeling, a temperature dependency of the QLR parameter has to be introduced. This is not yet done in the EKV3 model.

Concerning the narrow width effect (NWE), we observe that PMOS present an inverse narrow width (INWE) effect due to shallow trench isolation (STI). As for the RSCE effect, a significant reduction of this INWE effect with temperature is observed. The INWE effect was not modeled in EKV2.6 but is modeled in EKV3 by using two parameters: WR and QWR. As for the RSCE effect, and in order to obtain a precise low temperature modeling, a temperature dependency of the QWR parameter has to be introduced. In NMOS transistors, we observed an anomalous narrow width effect. These transistors do not present a classical NWE effect, neither an INWE effect. To understand

this effect, complementary measurements were done at different bulk voltages. We observe that the threshold voltage shift DV_{th} is sensitive to the bulk voltage. This anomalous NWE effect is not modeled in the EKV3 compact model.

In some 1.8 V LVT NMOS transistors, we observed a peak in the gate transconductance characteristic, G_m vs. V_{gs} , at temperature lower than 200 K. This peak is observed at the beginning of strong inversion, only on long channels and not on transistors shorter than 2 μm . It is not observed on 1.8 V STD transistors, even with long channels. To understand this phenomenon, complementary measurements were done by varying the bulk voltage V_{bs} . The peak-to-valley ratio in G_m is attenuated and tends to unity as V_{bs} increases. Such a peak has been already observed at intermediate temperature (77-120 K) on some CMOS processes [6]. It could be interpreted as the result of quantization effects in the inversion layer. Energy subband separation effects are enhanced at very low temperature or at very high effective transverse field E_{eff} at the Si/SiO₂ interface. At temperature not too low, different subbands with different mobility are filled. The occupancy of these subbands is modified by E_{eff} . As E_{eff} is proportional not only to the inversion charge Q_i but also to the depletion charge Q_b , subbands occupancy can also be varied by the channel doping N_{ch} or by the bulk voltage. In order to observe the peak in the G_m vs. V_{gs} characteristic, the first subband must be filled. So the temperature must not be too low, otherwise only the fundamental subband will be filled. The effective transverse electrical field must also be low. This last condition is achieved for low V_{gs} (low Q_i), and/or low N_{ch} or low V_{bs} (low Q_b). This interpretation is consistent with the fact that we observe this phenomenon only on low doped transistors, i.e. on LVT transistors, and not on STD transistors where the channel doping is higher. It is also coherent with the fact that we observe it only on long channel. As a matter of fact, due to the RSCE effect existing in these transistors, the effective channel doping increases as the channel length decreases and the G_m peak is no more observed. This quantum mechanical effect is not modeled in any advanced compact models, such as EKV3, PSP or HiSIM.

A carrier freeze-out effect in the LDD regions is observed on some 3.3 V transistors at temperature lower than 150 K. This phenomenon leads to an important error when evaluating the drain conductance of short transistors at very low drain-to-source voltages (less than 250 mV) in strong inversion. Although LDD zones also exist in the 1.8 V transistors, we do not observe any freeze-out effects down to 77 K. This is probably due to the existence of highly doped pockets under the LDD zones in this technology. This carrier freeze-out effect in the LDD zones is not modeled in any advanced compact models. A quantitative model for the LDD resistance accounting for the field assisted impurity ionization process was described in ref. [7]. We found that this model fits well the experimental G_{ds} - V_{ds} characteristics at low V_{ds} .

The gate transconductance G_m measured in the ohmic mode ($V_{ds}=50$ mV) could be negative for cooled NMOS transistors at high vertical fields. The explanation is that, when increasing V_{gs} , the increase of the inversion charge could not compensate the high mobility attenuation. The drain current will decrease, so G_m becomes negative. The improved charge-based mobility model introduced in the EKV3 model allows to reproduce accurately drain current and gate transconductance in the linear regime for 1.8 V NMOS transistors of this technology.

In conclusion, the EKV3 compact MOSFET model was evaluated for simulation of mixed analog-digital circuits working in the temperature range 77-200 K. This model was successfully applied in all inversion regimes and over different geometries and temperatures on different transistors of a 0.18 μm CMOS process. An evolved mobility model, an improved model accounting for weak inversion slope degradation and modeling of different effects such as RSCE, INWE, Drain Induced Barrier Lowering (DIBL) and Drain Induced Threshold Voltage Shift (DITS) which are included in this model are necessary for precise analog modeling. Some specific effects, such as narrow channel effect, freeze-out in LDD zones and quantization effect, are observed at low temperature on some transistors and are not yet modeled. Further improvements of this model will allow a very precise description of MOS transistors at low temperature.

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