MOSFET Compact Modeling Issues for Low Temperature (77 K - 200 K) Operation

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ABSTRACT

Advanced compact models are evaluated for simulation of mixed analog-digital circuits working at low temperature (77 to 200 K). This evaluation is performed on a dual gate oxide CMOS technology with 0.18 µm / 1.8 V and 0.35 µm / 3.3 V MOSFET transistors. A detailed temperature analysis of some physical effects is performed. Specific effects, such as anomalous narrow width effect or quantization of the inversion charge, are observed at low or intermediate temperature. Some improvements of compact models will allow a very accurate description of MOS transistors at low temperature.

Keywords: MOSFET, compact model, low temperature

1 INTRODUCTION

This paper deals with the simulation of hybrid CMOS readout circuits working at low or at intermediate temperature, typically 77 K, 130 K or 200 K, such as those used in high performance infrared image sensors [1]. SPICE parameters of transistors, including DC, AC, 1/f noise and matching parameters, are mandatory for design and simulation of such circuits. However CMOS foundries do not provide full sets of MOSFET parameters for simulation at temperature lower than -55°C (≈ 220 K). So these MOSFET parameters must be extracted prior to circuit simulation. Furthermore, the used MOSFET compact model must address the important weak and moderate inversion regimes where most of the analog transistors of the CMOS readout circuits are operating. A low temperature version of the EKV2.6 model was previously described and was successfully applied to different CMOS bulk processes such as 0.7 µm / 5 V, 0.5 - 0.35 µm / 3.3 V and 0.21 µm / 1.8 V from different foundries at cryogenic temperature [2]. In particular this model incorporates a charge-based mobility model including Coulomb, phonon and surface roughness scattering mechanisms as well as velocity saturation.

In this work, we access different compact models, such as the standard version of the EKV3 charge model [3], for a commercial process, namely a dual gate oxide CMOS technology, with 0.18 µm / 1.8 V and 0.35 µm / 3.3 V MOSFET transistors.

2 CMOS PROCESS

We characterize a commercial mixed mode / RFCMOS process optimized for room temperature operation. In this dual gate oxide process, two kinds of MOSFET transistors are available: (1) transistors with a physical gate thickness of 3.3 nm, a minimum channel length of 0.18 µm and operating at a maximum recommended voltage of 1.8 V and (2) transistors with a physical gate thickness of 6.5 nm, a minimum channel length of 0.35 µm and operating at 3.3 V. p-MOSFET are made in a NWELL. Depending on the channel doping, transistors with different threshold voltages are provided. p-MOSFET transistors may be done either with a standard threshold voltage (STD) or with a low threshold voltage (LVT). n-MOSFET transistors are made either in a P-substrate (also referred as the PWELL) or in a triple well (TWELL). n-MOSFET transistors have either a standard threshold voltage (STD), a low threshold voltage (LVT) or a zero-volt threshold voltage (ZVT). As a whole, twelve MOSFET transistors are allowed for mixed analog-digital circuit design. This process is a dual gate process and uses two kinds of polysilicon gates, N^+ doped polysilicon gate for n-MOSFET and P^+ doped polysilicon gate for p-MOSFET. As a consequence both NMOS and PMOS are surface channel transistors and the threshold voltage temperature coefficients are nearly equal (0.8 ~ 1.2 mV/K). This deep submicron process has pocket implants to combat short channel effects. Finally we have to mention that this process has LDD zones to diminish hot-carrier degradation and use Shallow-Trench Isolation (STI).

3 CHARACTERIZATION

Prior to parameter extraction using a compact model, a fine characterization of the different transistors at different temperatures is needed. This step is mandatory to examine different effects, such as short channel and narrow width effects.

NMOS and PMOS present a reverse short channel (RSCE) effect and the Vth roll-up is observed (Fig. 1). The Vth roll-off due to both charge sharing and Drain Induced Barrier Lowering (DIBL) is not observed. The threshold voltage shift [DVth = Vth - Vth (L = 20 µm)] is rather insensitive to the bulk voltage Vbs.

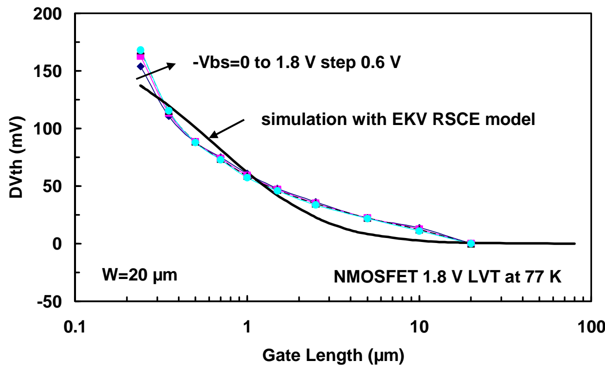

Figure 1: Measured RSCE threshold voltage shifts (symbols) and simulated curve (solid line)

A significant reduction of this RSCE effect with temperature is observed (Fig. 2). This reduction has been previously observed and interpreted as the variation of the threshold voltage with the Fermi potential [4]. The RSCE effect is well modeled in the EKV2.6 and EKV3 compact models at a given temperature as shown in Fig. 1 by using two parameters: LR and QLR, where LR is a characteristic length and QLR a charge density. In order to obtain a very precise low temperature modeling, a quadratic temperature dependency of the QLR parameter has to be introduced as shown in Fig. 3.

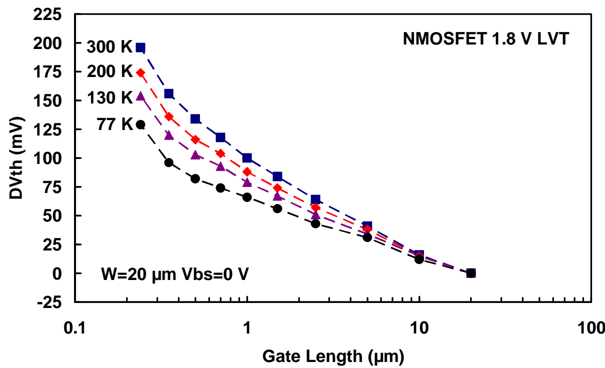

Figure 2: Measured RSCE threshold voltage shifts

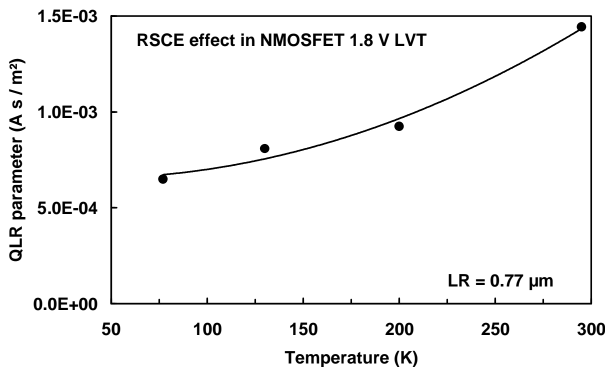

Figure 3: Variation of the QLR parameter with temperature

Concerning the narrow width effect (NWE), PMOS transistors of this process present an inverse narrow width (INWE) effect due to shallow trench isolation (STI). A significant change of this INWE effect with temperature is observed (Fig. 4). As for the RSCE effect, and in order to obtain a precise low temperature modeling, a temperature dependency of this effect has to be introduced.

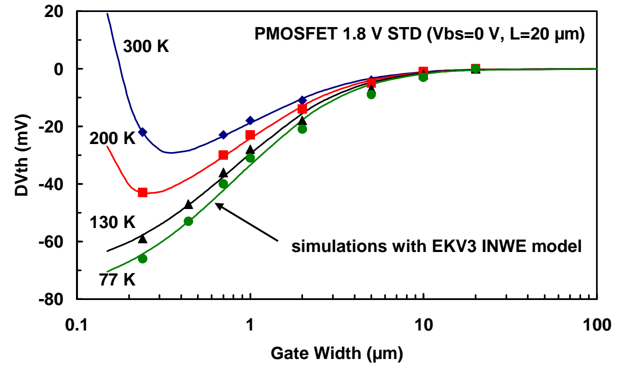

Figure 4: INWE effect at different temperatures: experimental (symbols) and simulated curves (solid lines)

In NMOS transistors, we observed an anomalous narrow width effect (Fig. 5). These transistors do not present a classical NWE effect, neither an INWE effect. The threshold voltage shift DVth is sensitive to the bulk voltage. This anomalous NWE effect is not modeled in the EKV3 compact model.

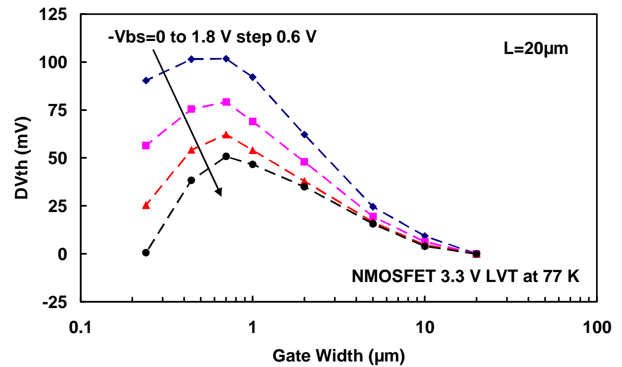

Figure 5: Anomalous NWE effect at 77 K

In lowly doped 1.8 V LVT NMOS transistors, we observed a peak in the gate transconductance characteristic, Gm vs. Vgs, at temperature lower than 200 K (Fig. 6). This peak is observed at the beginning of strong inversion. It is observed only on long channels and not on transistors shorter than 2 µm (Fig. 7). It is not observed on 1.8 V STD transistors, even with long channels.

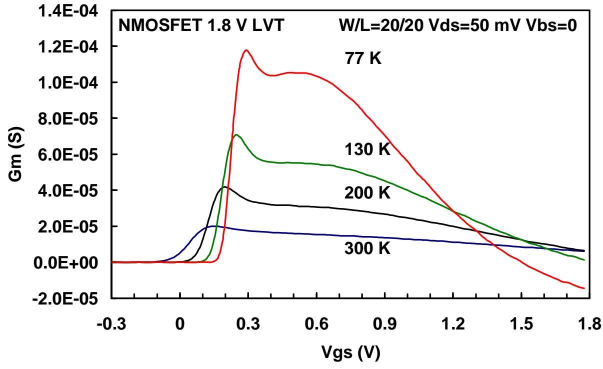

Figure 6: Gm behavior at different temperatures for a long channel 1.8 V LVT NMOSFET

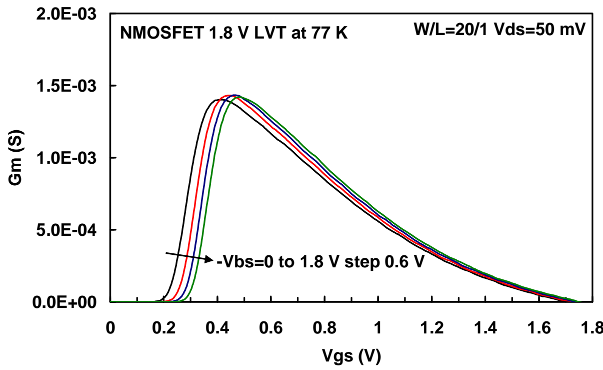

Figure 7: Gm behavior at 77 K for a short channel transistor

To understand this phenomenon, complementary measurements were done by varying the bulk voltage (Fig. 8). As shown in Fig. 9, the peak-to-valley ratio in Gm is attenuated and tends to unity as the bulk voltage increases.

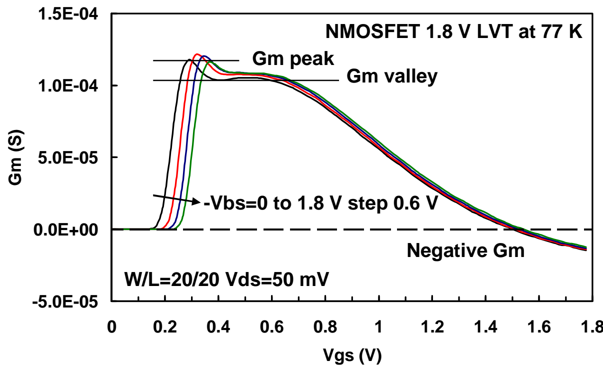

Figure 8: Gm behavior at different Vbs

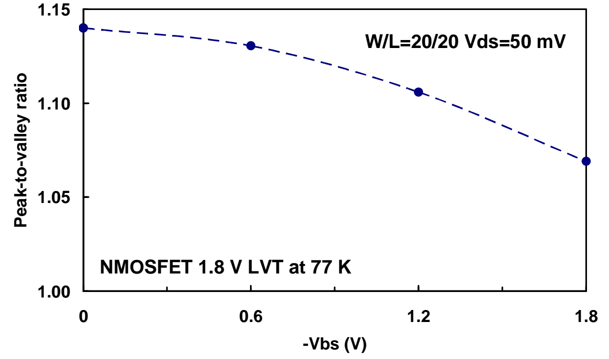

Figure 9: Gm peak-to-valley ratio vs. Vbs

Such a peak has been already observed at intermediate temperature (77 – 120 K) on some CMOS processes [5]. It has been interpreted as the result of quantization effects in the inversion layer. Energy subband separation effects are enhanced at very low temperature or at very high effective transverse field E_{eff} at the Si/SiO_2 interface given by:

$$E_{eff} = \frac{\eta\, Qi + Qb}{\varepsilon_{Si}} \qquad (1)$$

Where Qi is the inversion charge and Qb the bulk charge, η = 1/2 for NMOS and 1/3 for PMOS.

At not too low temperature, different subbands with different mobility are filled. The occupancy of these subbands is modified by E_{eff}. As E_{eff} is proportional not only to the inversion charge Qi but also to the depletion charge Qb, subbands occupancy can also be varied by the channel doping Nch or by the bulk voltage as Qb is given by eq. 2:

$$Qb = \sqrt{2\, q\, \varepsilon_{Si}\, Nch\, (\psi_s + Vsb)} \qquad (2)$$

In order to observe the peak in the Gm vs. Vgs characteristic, the first subband must be filled. So the temperature must not be too low, otherwise only the fundamental subband will be filled. The effective transverse electrical field must also be low. This last condition is achieved for low Vgs (low Qi), and/or low Nch or low Vbs (low Qb). This interpretation is consistent with the fact that we observe this phenomenon only on low doped transistors, i.e. on LVT transistors, and not on STD transistors where the channel doping is higher. It is also coherent with the fact that we observe it only on long channel. As a matter of fact, due to the RSCE effect existing in these transistors (see Fig. 1), the effective channel doping increases as the channel length decreases and the Gm peak is no more observed. This quantum mechanical effect is not taken into account in any advanced compact models, such as EKV3, PSP or HiSIM.

Another specific effect was observed. We found that as temperature is lowered, the measured subthreshold swing of long transistors is higher than that predicted by simulation. This is due to interface traps whose density Nit increases when temperature decreases. In the EKV3, an empirical parameter N0 is introduced, having an ideal value of N0 = 1, corresponding to the absence of interface states. This parameter, which does not affect the strong inversion regime, allows minimizing the error in weak inversion (Fig. 10).

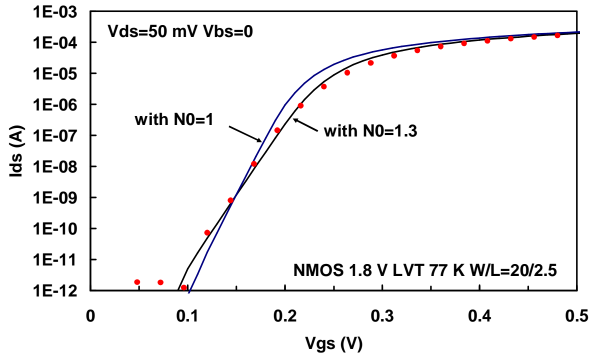

Figure 10: Influence of interface traps on the subthreshold slope, experimental (symbols) and EKV3 simulations (solid lines) at 77 K

As shown in Fig. 8, the gate transconductance measured in the ohmic mode (Vds = 50 mV) could be negative on cooled NMOS transistors at high vertical field. The explanation is that, when increasing Vgs, the increase of the inversion charge could not compensate the high mobility attenuation. The drain current will decrease, so Gm becomes negative. The improved charge-based mobility model introduced in the EKV3 model allows to reproduce accurately drain-source current and gate transconductance in the linear regime as shown in Fig. 11.

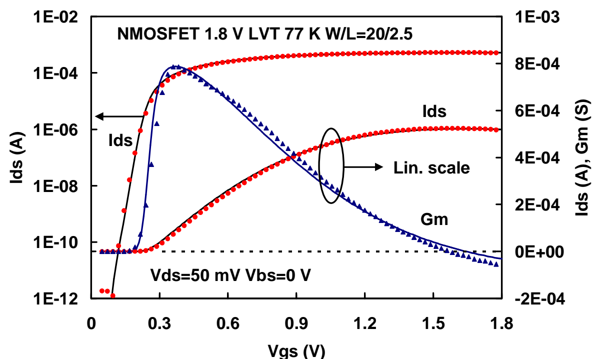

Figure 11: Experimental (symbols) and simulated (solid lines) drain-source current (Ids) and gate transconductance (Gm) with EKV3 at 77 K

4 CONCLUSION

In conclusion, better MOSFET compact models with new mobility law and accounting for weak inversion slope degradation due to interface traps and for different effects such as RSCE, INWE, DIBL and DITS (Drain Induced Threshold Voltage Shift) are necessary for precise analog modeling at low temperature. Specific effects, such as anomalous narrow width or quantization effects, observed only in some transistors, are not yet well understood. It is expected that further improvements will allow a very accurate MOSFET modeling at low temperature.

5 ACKNOWLEDGEMENTS

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REFERENCES

[1] F. Guellec, P. Villard, F. Rothan, L. Alacoque, C. Chancel, P. Martin, P. Castelein, P. Maillart, F. Pistone and P. Costa, “Sigma-delta Column-wise A/D Conversion for Cooled ROIC”, SPIE Proceedings Vol. 6542, Infrared Technology and Applications XXXIII, 2007.

[2] P. Martin and M. Bucher, “Comparaison of 0.35 and 0.21 µm CMOS Technologies for Low Temperature Operation (77 K - 200 K) and Analog Circuit Design”, 6th Workshop on Low Temperature Electronics (WOLTE-6), ESTEC, Noordwijk, The Netherlands, 2004.

[3] A. Bazigos, M. Bucher, F. Krummenacher, J.-M. Sallese, A.-S. Roy, C. Enz, “EKV3 Compact MOSFET Model Documentation, Model Version 301.01”, Technical Report, Technical University of Crete, November 23, 2007.

[4] B. Szelag, F. Balestra and G. Ghibaudo, “Comprehensive Analysis of Reverse Short-Channel Effect in Silicon MOSFET’s from Low-Temperature Operation”, IEEE Electron Devices Letters, vol. 19, n° 12, pp. 511-513, 1998.

[5] A. Emrani, “Propriétés électriques et modèles physiques des composants MOS à basse température pour la cryo-microélectronique”, PhD Thesis, INPG, Grenoble, 1992.