Explicit 2D Compact Model of Independent Double Gate MOSFET

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Abstract - This paper describes an explicit 2D threshold voltage based compact model of Independent Double Gate (IDG) MOSFET with undoped channel. The validity of this model is demonstrated by comparison with Atlas simulations. The model was implemented in circuit simulator in VerilogA language to design digital and analog circuits using the independent gate structures.

I Introduction

IDG MOSFET is a particularly promising device, which is expected for sub-32nm node. To take advantage of the second gate, which can be independently driven and to design new circuits, a compact model including Short Channel Effects (SCE) is crucial.

For the first time, an explicit 2D compact model of IDG MOSFET is presented. The model is a threshold-voltage (V_{th}) based compact model. We first explain the compact model in the case of a long transistor. Then, we show how short channel effects are added in the core of the model. Finally, the model is implemented in simulator in VerilogA language and validity is demonstrated by confrontation with Atlas numerical simulations [1].

II Explicit V_{th} model for a long device

Fig. 1 shows the device structure. L is the gate length, T_{si} the silicon film thickness (10 nm), $T_{ox1,2}$ the front and back gate oxide thicknesses (1nm). $V_{g1,2}$ are the front and back gate voltages. Without generality loss, $\Delta\Phi_{m1,2}$ the work function differences between the front and the back gate and the intrinsic silicon are supposed null.

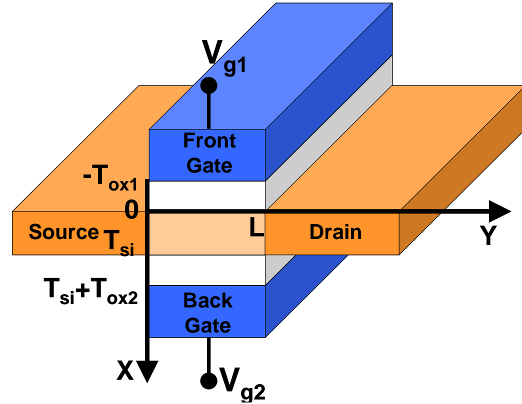

Fig. 1: An IDG MOSFET.

In [2], explicit drain current I_{ds} is given as:

$$I_{ds} = I_{ds1} + I_{ds2} \quad (1)$$

$$I_{ds1} = \frac{W}{L}\mu\, C_{ox1}\, V_{gt1,eff}\left(1 - n_{1,eff}\frac{V_{ds1,eff}}{2\left(V_{gt1,eff} + 2u_t\right)}\right)V_{ds1,eff} \quad (2a)$$

$$I_{ds2} = \frac{W}{L}\mu\, C_{ox2}\, V_{gt2,eff}\left(1 - n_{2,eff}\frac{V_{ds2,eff}}{2\left(V_{gt2,eff} + 2u_t\right)}\right)V_{ds2,eff} \quad (2b)$$

Where W is the gate width, μ the mobility (assumed constant), u_t the thermal voltage and, C_{oxj} the front and the back gate oxide capacitances respectively. Index j is 1 or 2. $V_{gtj,eff}$ represent the effective gate voltages. They unify weak and strong inversion thanks to an analytical threshold voltage, which takes into account the coupling between both front and back interfaces. $n_{j,eff}$ are the effective coupling factors. $V_{dsj,eff}$ correspond to the effective drain voltages. They allow a good modeling of the drain saturation voltage. All these parameters are analytical and explicit.

III Explicit SCE model

2D Poisson equation is analytically solved in weak inversion. The evanescent-mode analysis is used as in [3] to get the channel potential distribution:

$$\psi(x,y) = \psi_{1D}(x) + \Delta\psi(\mathrm{x},\mathrm{y}) \quad (3a)$$

$$\Delta\psi(\mathrm{x},\mathrm{y}) = \frac{\mathrm{b}_1 \mathrm{sh}\left(\frac{\pi}{\lambda_1}(L-y)\right) + \mathrm{c}_1 \mathrm{sh}\left(\frac{\pi}{\lambda_1} y\right)}{\mathrm{sh}\left(\frac{\pi}{\lambda_1} L\right)} \cos\left(\frac{\pi}{\lambda_1} x\right) \quad (3b)$$

$\psi_{1D}(x)$ is the 1D surface potential and $\Delta\psi(x,y)$ the 2D correction term. λ_1, b_1 and c_1 are given in [3]; we are in the same assumptions.

Consequently, the drain current for a short channel device in weak inversion is expressed as:

$$I_{ds} = \mu W u_t \left(1 - \exp\left(-\frac{V_{ds}}{u_t}\right)\right) \frac{1}{\int_0^L \frac{dy}{\int_{-\frac{T_{si}}{2}}^{\frac{T_{si}}{2}} q.n_i \exp\left(\frac{\psi(x,y)}{u_t}\right) dx}} \quad (4)$$

V_{ds} is the drain voltage, q the electronic charge and n_i the intrinsic carrier concentration. Due the double integral, this expression can not be considered as explicit. In order to obtain an explicit compact model, we assume that for the correction term, the current mainly flows in x_{max}, the maximum potential in the x direction and in y_{min}, the minimum potential in the y direction. It is the point where the electron density is maximal. x_{max} and y_{min} are obtained when the respective derivative is zero. Thus, we get the following explicit expression of I_{ds} in weak inversion:

$$I_{ds} = -\mu \frac{W}{L} q\, n_i\, T_{si}\, u_t^2 \frac{\exp\left(\frac{\psi_{s1}}{u_t}\right) - \exp\left(\frac{\psi_{s2}}{u_t}\right)}{(\psi_{s1} - \psi_{s2})} \exp\left(\frac{\Delta\psi(x_{\max}, y_{\min})}{u_t}\right)\left(\exp\left(-\frac{V_{ds}}{u_t}\right) - 1\right) \quad (5)$$

$$\mathrm{x}_{\max} = \frac{\lambda_1}{\pi} \arcsin\left(\frac{\lambda_1}{\pi} \frac{sh\left(\frac{\pi L}{\lambda_1}\right)}{\sqrt{2 b_1 c_1 ch\left(\frac{\pi L}{\lambda_1}\right) - b_1^2 - c_1^2}}\right) \quad (6a)$$

$$\mathrm{y}_{\min} = \frac{\lambda_1}{\pi} \ln\left(\frac{\frac{b_1}{c_1}\exp\left(\frac{\pi L}{\lambda_1}\right) - 1}{1 - \frac{b_1}{c_1}\exp\left(-\frac{\pi L}{\lambda_1}\right)}\right) \quad (6b)$$

ψ_{s1} and ψ_{s2} are the front and the back gate surface potentials, derived considering the DG MOSFET as a capacitive divider. Thus,

$$\Delta\psi(x_{\max}, y_{\min}) = \frac{\sqrt{2.b_1.c_1 \cosh\left(\pi \frac{L}{\lambda_1}\right) - b_1^2 - c_1^2}}{\sinh\left(\pi \frac{L}{\lambda_n}\right)} \cos\left(\arcsin\left(\frac{\lambda_1}{\pi} \frac{sh\left(\frac{\pi L}{\lambda_1}\right)}{\sqrt{2 b_1 c_1 ch\left(\frac{\pi L}{\lambda_1}\right) - b_1^2 - c_1^2}}\right)\right) \quad (7)$$

Eq. (5) could be written as the sum of I_{ds1} and I_{ds2} with I_{dsj} given by:

$$I_{dsj} = -\mu \frac{W}{L} n_j c_{oxj} u_t^2 \left(e^{\left(-\frac{V_{ds}}{u_t}\right)} - 1\right) e^{\left(\frac{V_{gj} - V_{thj}}{n_j u_t}\right)} e^{\left(\frac{\Delta\psi(x_{\max}, y_{\min})}{u_t}\right)} \quad (8)$$

V_{thj} is the 1D threshold voltage and n_j the 1D coupling factor. To include SCE in our compact model, we want to express I_{dsj} as:

$$I_{dsj} = -\mu \frac{W}{L} n_j\, c_{oxj}\, u_t^2 \left(e^{\left(-\frac{V_{ds}}{u_t}\right)} - 1\right) e^{\left(\frac{V_{gj} - V_{thj,sce}}{n_{j,sce}\, u_t}\right)} \quad (9)$$

The 2D threshold voltages $V_{thj,sce}$ and coupling factors $n_{j,sce}$ will be obtained by identification of (7) and (8). Then, expressions (10a, b, c, d and e) and (11) are obtained.

$$V_{thj,sce} = V_{thj} + \frac{-b+\sqrt{\Delta}}{2a} \tag{10a}$$

$$a = \frac{1}{n_j^{\,2}} sh^2\left(\frac{\pi L}{\lambda_1}\right) - \frac{\chi^2}{2}\left[ch\left(\frac{\pi L}{\lambda_1}\right) - 1\right] \tag{10b}$$

$$b = \chi^2\left(2\left(\frac{E_g}{2} - \frac{V_{thj}+V_{gj'}}{2}\right) + V_{ds}\right)\left[ch\left(\frac{\pi L}{\lambda_1}\right) - 1\right] \tag{10c}$$

$$c = -2\chi^2\left(\frac{E_g}{2} - \frac{V_{thj}+V_{gj'}}{2}\right)\left(\frac{E_g}{2} - \frac{V_{thj}+V_{gj'}}{2} + V_{ds}\right)\left[ch\left(\frac{\pi L}{\lambda_1}\right) - 1\right] + V_{ds}^{2} \tag{10d}$$

$$\chi = \frac{2\lambda_1^{\,2}\tan\left(\pi\frac{T_{oxj}}{\lambda_1}\right)\sin\left(\pi\frac{T_{si}}{2\lambda_1}\right)}{\pi^2 T_{oxj}\left[\frac{T_{si}}{2} + \frac{\sin\left(\pi\frac{T_{si}}{\lambda_1}\right)}{\sin\left(\pi\frac{T_{oxj}+T_{oxj'}}{\lambda_1}\right)}T_{oxj}\right]} \tag{10e}$$

E_g is the energy gap. j' represents the opposite gate: if j=1 (for the front gate), so j'=2 (for the back one) and if j=2 then j'=1.

$$n_{1,sce} = \frac{1}{\frac{1}{n_1} + \frac{\chi\left(1 - ch\left(\frac{\pi L}{\lambda_1}\right)\right)\left(\frac{E_g}{2} + \frac{V_{ds}}{2} - \frac{V_{th1,sce}+V_{g2}}{2}\right)}{sh\left(\frac{\pi L}{\lambda_1}\right)\sqrt{\left(ch\left(\frac{\pi L}{\lambda_1}\right) - 2\right)\left(\frac{E_g}{2} - \frac{V_{th1,sce}+V_{g2}}{2}\right)\left(\frac{E_g}{2} + V_{ds} - \frac{V_{th1,sce}+V_{g2}}{2}\right)}}} \tag{11}$$

These 2D expressions are replaced in (2a) and (2b) to get a unified model.

We also add an expression of the early voltage (BSIM like) to take into account the channel length modulation.

IV Implementation and Results

This compact model was written in VerilogA to allow simulations with Eldo (Mentor Graphics) or ADS (Agilent) circuit simulators. Comparisons between Atlas and ADS simulations of I_{ds} for the symmetrical case are shown in Fig. 2 and 3.

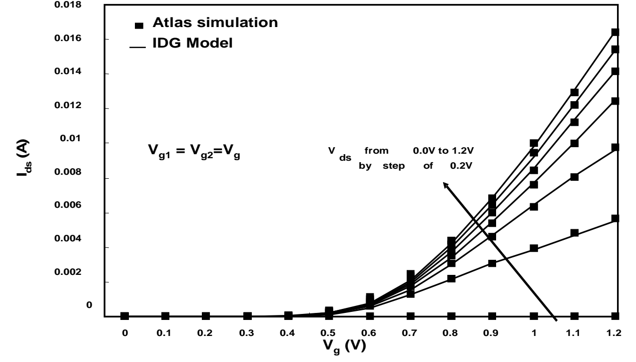

Fig. 2: Drain current versus gate voltage for several drain voltage.

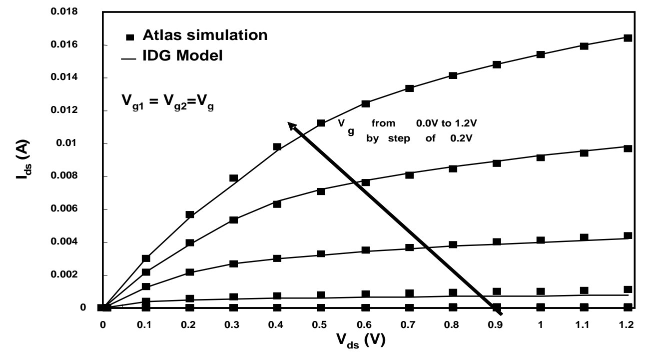

Fig. 3: Drain current versus drain voltage for several gate voltages.

For the case when the gates are independently driven, results are exposed on Fig. 4 to 7 for a short channel device L=30nm (W=1µm).

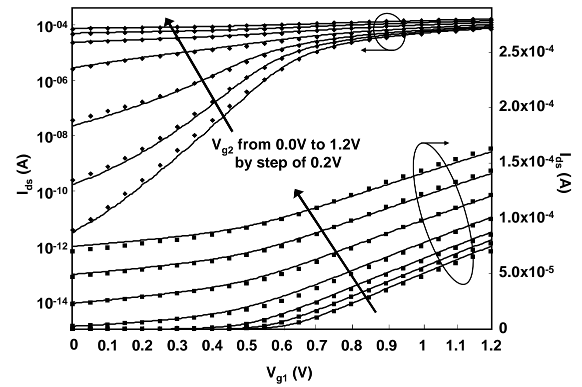

Fig. 4: Drain current versus front gate voltage for several back gate voltages at low drain voltage (V_{ds}=5mV) in logarithmic and linear scales.

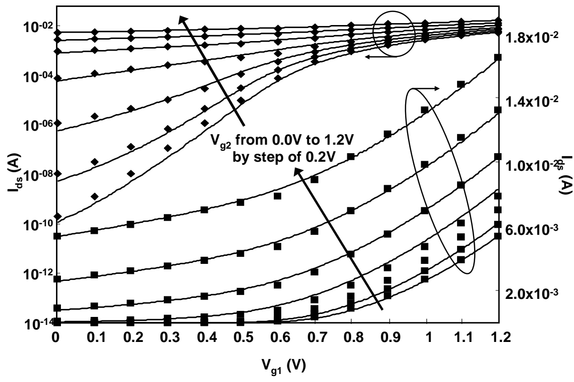

Fig. 5: Drain current versus V_{g1} for several V_{g2} at V_{ds}=1.2V.

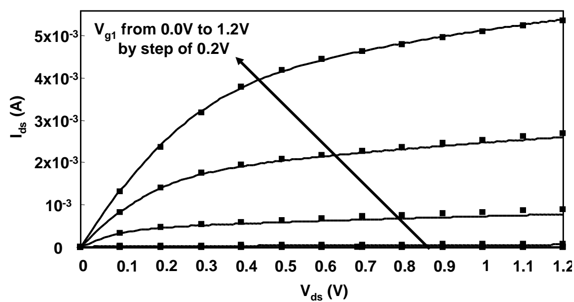

Fig. 6: Drain current versus V_{ds} for several V_{g1} at V_{g2}=0.0V.

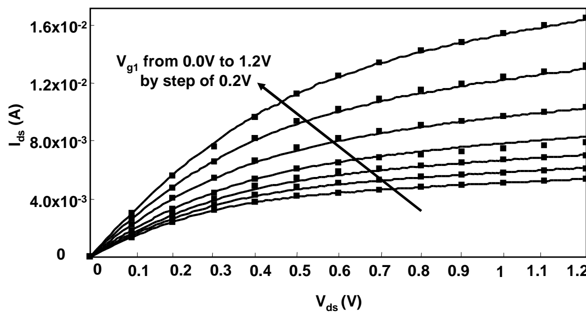

Fig. 7: Drain current versus V_{ds} for several V_{g1} at V_{g2}=1.2V.

Our 2D compact model of IDG MOSFET agrees very well with Atlas simulations. That proves the accuracy and the validity of this model.

Moreover, the drain conductance is compared to Atlas simulations in Fig. 8.

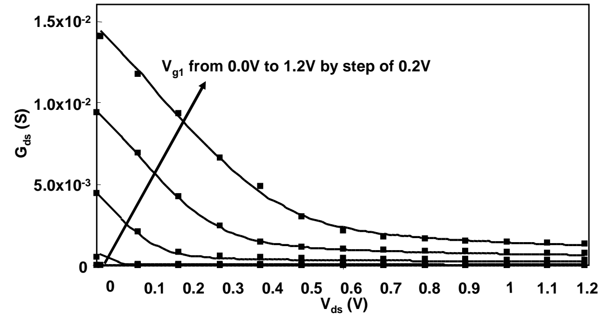

Fig. 8: Drain conductance versus V_{ds} for several V_{g1} at V_{g2}=0.0V.

This proves again the good accuracy of our new compact model.

V Conclusion

An explicit compact model of IDG MOSFET with SCE was presented. This new model was written in VerilogA and implemented in Eldo and in ADS. Atlas and ADS simulations were confronted and prove the accuracy of our model. Not only the drain current model agrees very well with numerical Atlas simulations, but also the drain conductance.

References

[1] ATLAS User's Manual – Device Simulation Software, SILVACO International Inc.

[2] M. Reyboz, T. Poiroux, O. Rozeau, P. Martin and J. Jomaah, "Explicit threshold voltage based compact model of independent double gate MOSFET", NSTI Nanotech, WCM, 2006.

[3] X. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs", IEEE Transac. On Electron Devices, vol.51, n°8, 2004.