Explicit Compact Model of Independent Double Gate MOSFET

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I Abstract

This paper describes an explicit compact model of Independent Double Gate (IDG) MOSFET with undoped channel. The validity of this model is demonstrated by comparisons with Atlas simulations. The model was implemented in VerilogA in order to test it and to design circuits. Circuit results of a mixer and an inverter are presented.

II Introduction

DG MOSFETs are promising devices because they can be scaled to the shortest channel length, particularly IDG MOSFETs because they enlarge the circuit design space. That is why a compact model is crucial to take advantage of this new technology. However, explicit IDG MOSFET compact model does not really exist. Indeed, existing models require numerical resolutions or are not valid in all operating modes: [1]-[4]. This article shows a threshold voltage based model of IDG MOSFET. The model was validated by confrontation with numerical simulations [5]. It was implemented in VerilogA to design circuits. Circuit simulation results are presented to check its robustness.

III V_{th} model

Figure 1 shows the device. 1D Poisson equation is solved to derive the drain current I_{ds} with Boltzmann statistics. Boundary conditions, electrical neutrality and physical assumptions allow getting explicit I_{ds}. The inversion charge Q_{inv} was expressed as the sum of two inversion charges: Q_{inv1} and Q_{inv2}. When front and back interfaces are in weak inversion, the transverse electric field is uniform since the channel is assumed undoped. When both interfaces are in strong inversion, both inversion charges are independent since front and back interfaces are de-coupled. And if one interface is in strong inversion and the other one in weak inversion, Q_{inv} is supposed to be equal to the strong inversion charge. Thus, explicit I_{ds} is given as:

$$I_{ds} = I_{ds1} + I_{ds2} \quad (1)$$

$$I_{ds1} = \frac{W}{L}\mu \cdot C_{ox1} \cdot V_{gt1,eff}\left(1 - n_{1,eff}\frac{V_{ds1,eff}}{2\left(V_{gt1,eff} + 2u_t\right)}\right)V_{ds1,eff} \quad (2)$$

$$I_{ds2} = \frac{W}{L}\mu \cdot C_{ox2} \cdot V_{gt2,eff} \cdot \left(1 - n_{2,eff}\frac{V_{ds2,eff}}{2\left(V_{gt2,eff} + 2u_t\right)}\right)V_{ds2,eff} \quad (3)$$

W is the gate width, μ is the mobility, Φ_{imref} is the quasi Fermi level of electrons in the channel, u_t is the thermal voltage and $C_{ox1,2}$ are the front and the back gate oxide capacitances. $V_{gti,eff}$ represent the effective gate voltages. They allow continuity between weak and strong inversion thanks to a defined threshold voltage, which takes into account interface coupling between front and back interfaces. $n_{i,eff}$ are the effective coupling factors and $V_{dsi,eff}$ are the effective drain voltages, which allow a well modeling of the drain saturation voltage thanks to interface coupling. Moreover, short channel effects (SCE) are included in this model, but are not shown. Figures 2, 3, 4 and 5 present the comparison between Atlas simulations and the compact model. Finally, thanks to a charge model, AC and transient simulations were done.

IV Model validation on basic designs

This compact model was implemented in VerilogA to allow simulations under Eldo (Anacad) or ADS (Agilent) software. Simulation results of a mixer and an inverter are presented on Figures 6 and 7 to illustrate the robustness of this model.

V Conclusion

In this work, an explicit compact model was developed for undoped IDG MOSFET, which is valid for all operating modes. Comparisons with Atlas simulations verify the validity and accuracy of this model. Moreover, the model was implemented in VerilogA and circuits were simulated. The robustness of the model is excellent. This is demonstrated thanks to the simulation of a mixer and an inverter.

Acknowledgement

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References

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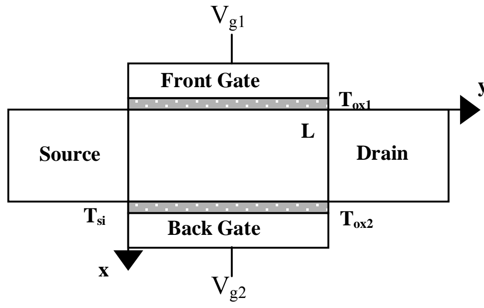

Figure 1: *ADG MOSFET, L is the gate length, T_{si} is the silicon film thickness (15 nm), T_{ox1} and T_{ox2} are the front and back gate oxide thicknesses. V_{g1} and V_{g2} are the front and back gate voltages. Without generality loss, $\Delta\Phi_{m1}$ and $\Delta\Phi_{m2}$ the work function differences between the front and the back gate and the intrinsic silicon are supposed null.*

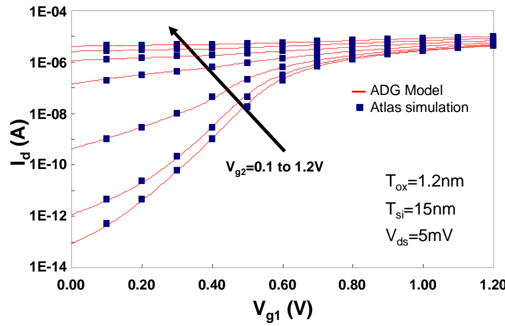

Figure 2: *Drain current versus front gate voltage for several back gate voltage values at low drain voltage (V_{ds}=5Mv) in logarithmic representation. L=0.5µm and W=1µm.*

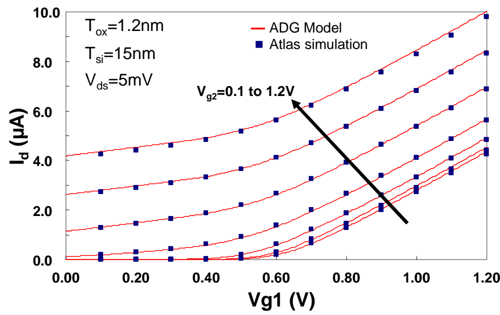

Figure 3: *Drain current versus front gate voltage for several back gate voltage values at low drain voltage (V_{ds}=50Mv) in linear representation. L=0.5µm and W=1µm.*

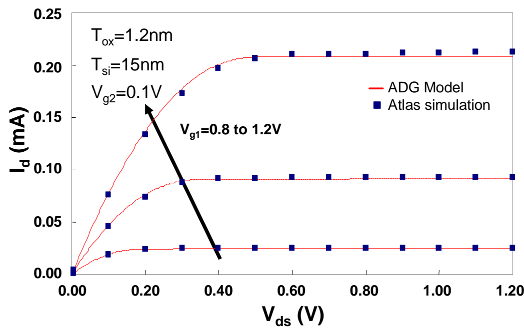

Figure 4: *Drain current versus drain voltage for several front gate voltage values at low back gate voltage (V_{g2}=0.1V). L=0.5µm and W=1µm.*

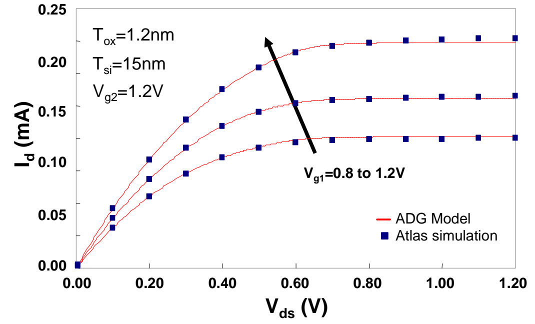

Figure 5: *Drain current versus drain voltage for several front gate voltage values at high back gate voltage (V_{g2}=1.2V). L=0.5µm and W=1µm.*

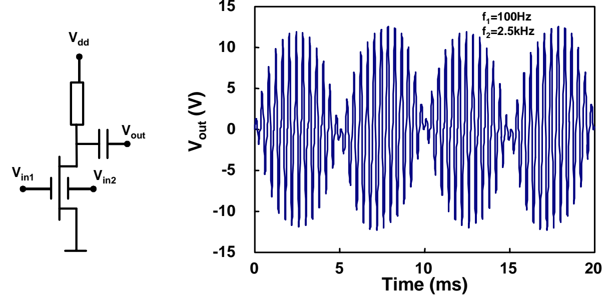

Figure 6a and 6b: *Schematic of a basic mixer and simulation results.*

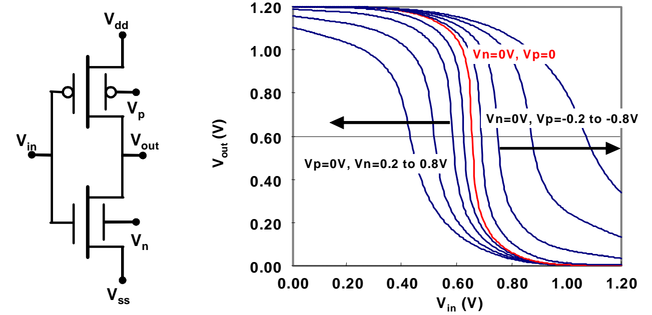

Figure 7a and 7b: *Schematic of an inverter and simulations with back gate voltage control using ADG compact model. Ln=Lp=1µm, Wn=5µm and Wp=10µm.*