# MOSFET Modeling for Low Temperature Analog Circuit Design

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# Acknowledgements


- Christian Enz
- Pioneering work of F. Théodoloz (EPFL)
- Matthias Bucher
- Analog designers from LETI : J.L. Martin, F. Rothan, …
- Ch. Chancel for experimental support
- French Ministry of Defense and CEA

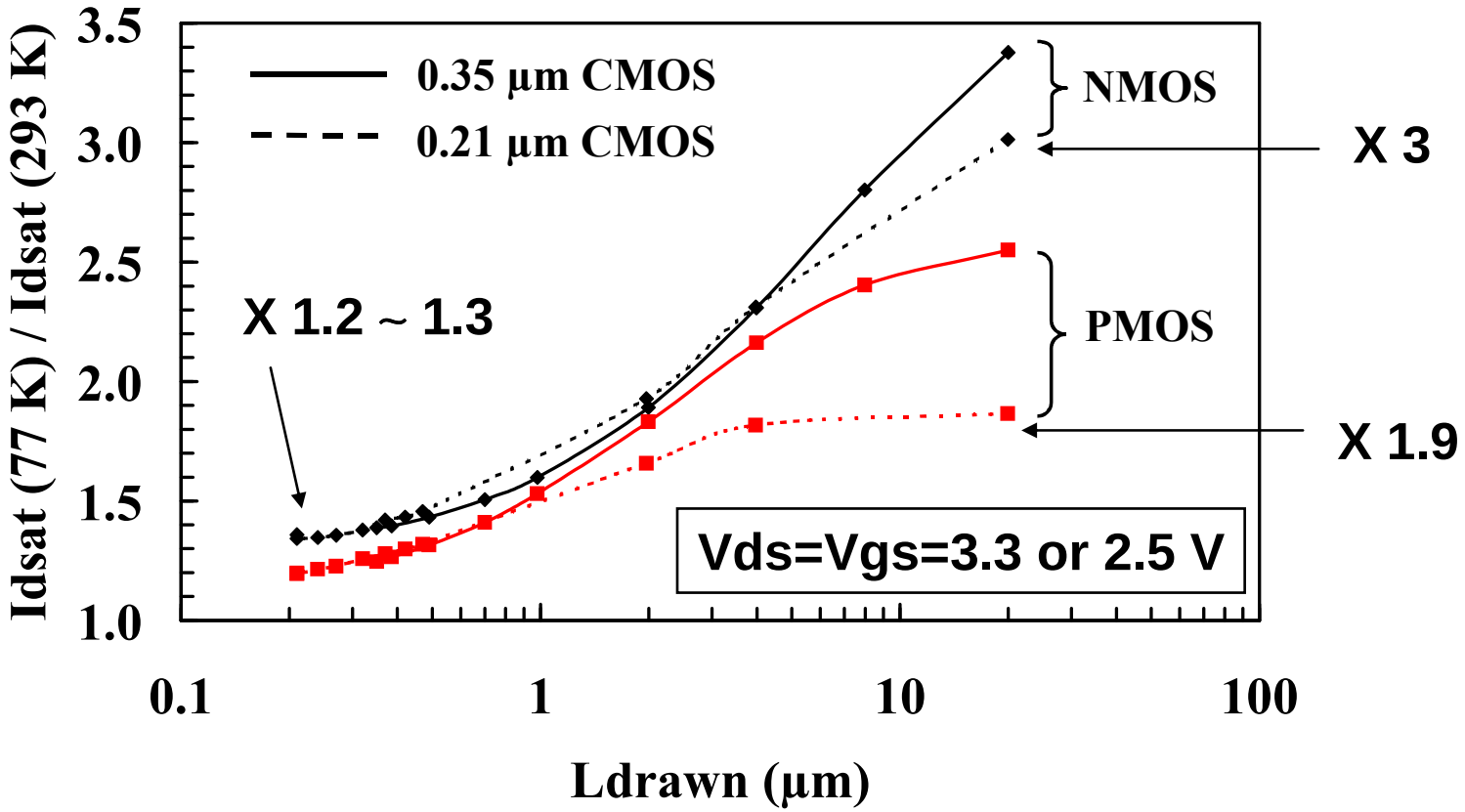
# Outline of presentation

- Why CMOS at low temperature ?
- Some studied CMOS processes at LT
- Compact MOSFET model for analog circuit design
- Examples of simulation
- Low frequency noise
- Transistor matching
- Summary and conclusion

**Keywords: analog MOSFET, weak & moderate inversion, low temperature, low frequency noise, transistor matching**

# Why CMOS at LT ? Higher saturation drain current ?

## Idsat 77 K / Idsat 293 K vs. drawn length




⇒ **Velocity saturation is the main effect limiting short-channel devices performance at LT**

# Saturation drain current

$$E < E_{crit}: \quad I_{d,sat} = \frac{1}{2} \mu C_{OX} \frac{W}{L} (Vg - Vt)^2$$

$$E > E_{crit}: \quad I_{d,sat} = C_{OX} W v_{sat} (Vg - Vt)$$

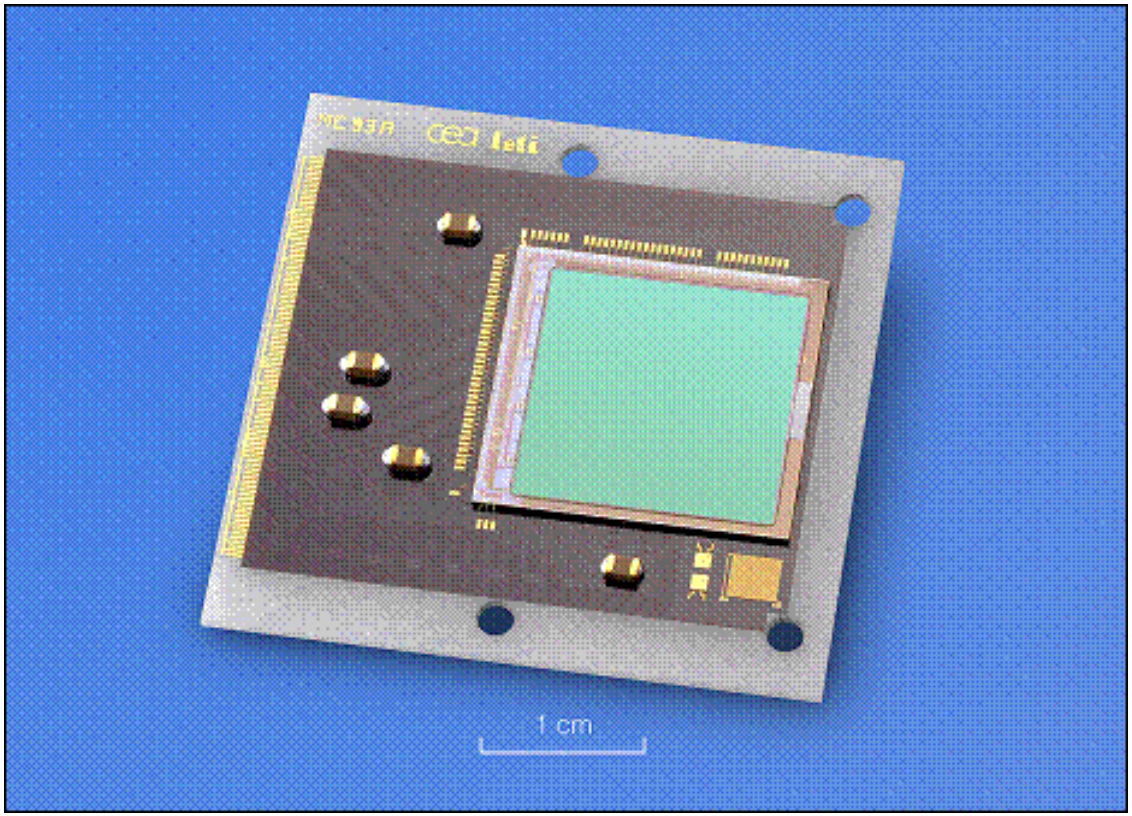
$E_{crit} \approx 5 \times 10^3$ V/cm at 300 K
$v_{sat} \approx 10^7$ cm/s at 300 K
$v_{sat}$ 77 K / $v_{sat}$ 300 K ≈ 1.2-1.3

# So why CMOS at LT ?

- **Design of infrared image sensors [ high performance, high complexity (1 Mpixel), 77 K – 200 K ]**
- **Simulation of hybrid CMOS analog read-out circuits**
- **No SPICE parameters at LT from CMOS foundries**
- **Validity of BSIM3v3 (Berkeley), EKV 2.6 (EPFL), MM9 (Philips) at T < 200 K ?**
- **Importance of weak - moderate inversion regimes**
- **Need to develop a specific analog model and extract DC, AC, 1/f noise and matching parameters**

# IRCMOS circuits designed at CEA-LETI

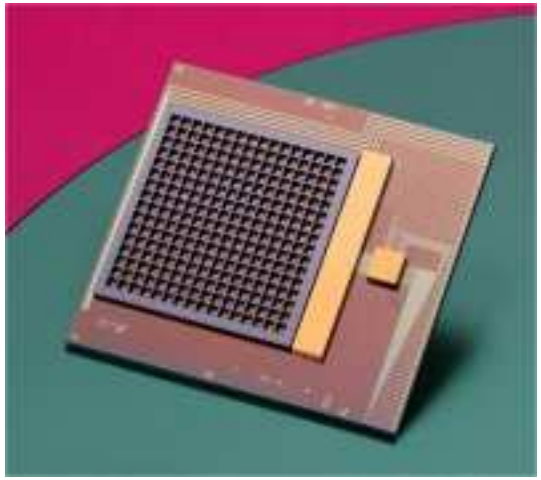
**IRCMOS 77 K**




**1024 x 1024 pitch 15 µm**

**Hybridisation by indium bumps**

**Herschel /PACS 0.3 K**



# CEA-LETI 1024 x 1024 MW-IRFPA p=15 µm T=77 K

# Studied CMOS processes (1/2)

➢ **0.7 µm - 5 V standard CMOS process:**

- **Single gate process ($N^+$ poly-Si ):**
  - **NMOS: surface channel (TCV_N ≈ 1 mV/K)**
  - **PMOS: buried channel (TCV_P ≈ 2 mV/K)**
- **AeroSense, SPIE Symposium (Orlando 2001)**

➢ **0.5 µm - 3.3 V standard CMOS process:**

- **Single gate process ($N^+$ poly-Si )**

# Studied CMOS processes (2/2)

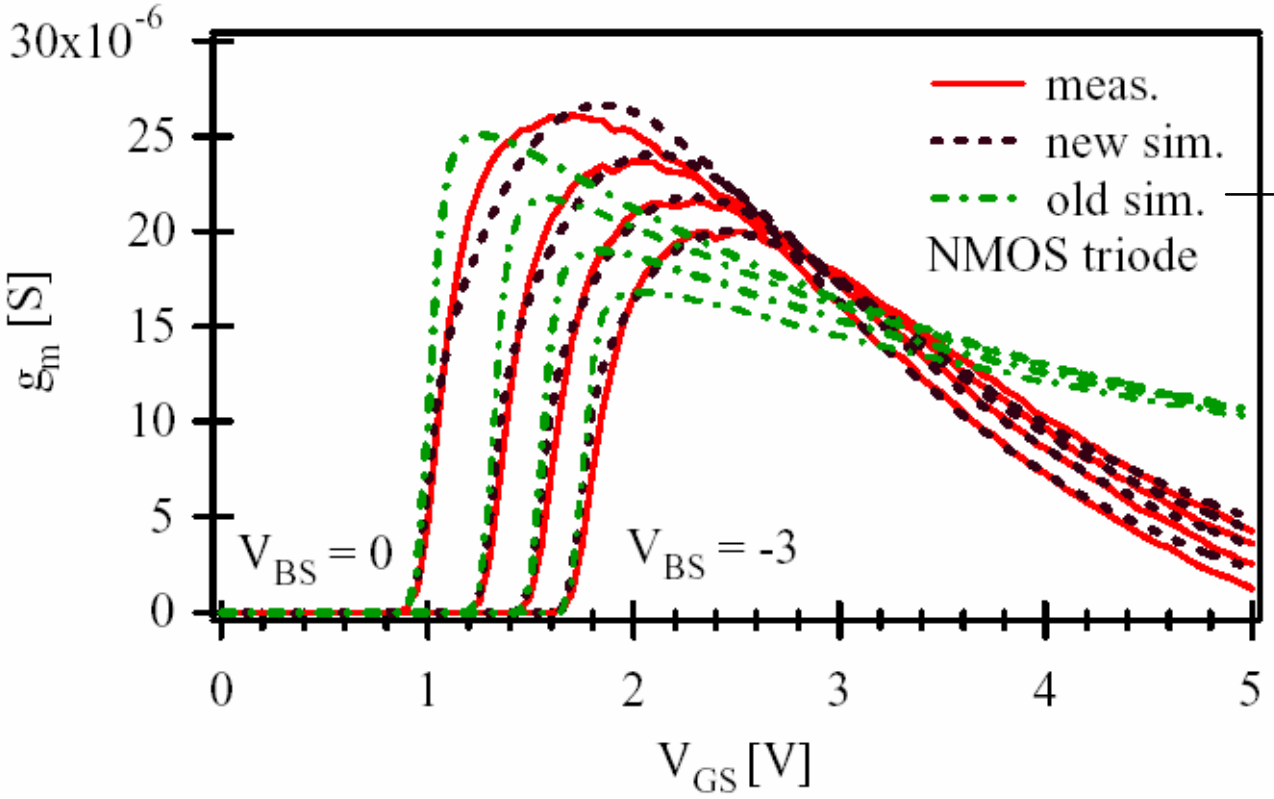
➢ **0.35 µm - 3.3 V standard CMOS process:**

- **Single gate process ($N^+$ poly-Si ):**
  - **NMOS: surface channel (TCV_N ≈ 1 mV/K)**
  - **PMOS: buried channel (TCV_P ≈ 2 mV/K)**
- **WOLTE-5 (Grenoble 2002)**

➢ **0.21 µm - 1.8 V std. process:**

- **Dual gate process: NMOS & PMOS surf. channels only (TCV_N ≈ TCV_P ≈ 1 mV/K) + Pocket implants**
- **MIXDES (Lodz 2003) & WOLTE-6 (Noordwijk 2004)**

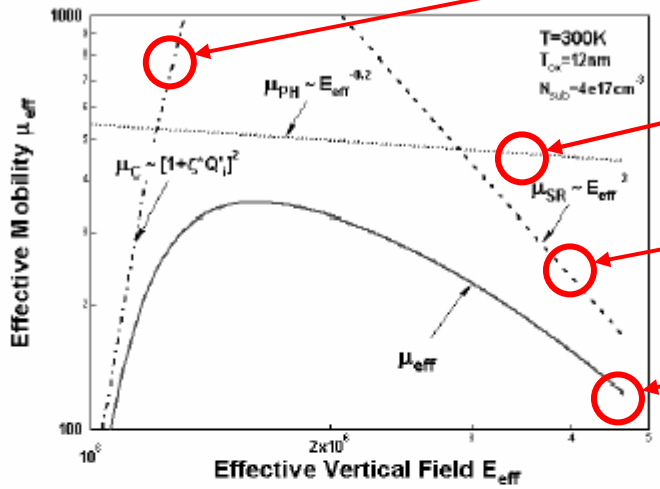
# The standard version of the EKV model at LT: main problem




→ **EKV 2.3 (THETA)**

**NMOS 77 K Tox=150 nm W/L=20/20 µm Vds=50 mV [1]**

# The standard version of the EKV model at LT: main problem

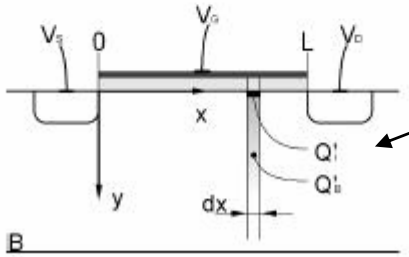



1/ Coulomb scatt.

2/ Phonon scatt.

3/ SR scatt.

Matthiessen




Qi = f(x), x = 0 → L

(From M. Bucher, CMC meeting, June 2004)

# The LT version of the EKV 2.6 model: main improvement

- New charge-based mobility model:

$$\mu = \frac{\mu_0}{\left(\frac{E_{eff}}{ECO}\right)^{-\alpha_1} + \left(\frac{E_{eff}}{EPH}\right)^{\frac{1}{3}} + \left(\frac{E_{eff}}{ESR}\right)^{2}} \qquad \text{with } E_{eff} = \frac{q\left(\eta Q_i + Q_b\right)}{\varepsilon_{Si}}$$

- 5 parameters: $\mu_0$, $\alpha_1$, ECO, EPH, ESR
- Local mobility $\rightarrow$ global mobility through integration along the channel

# Freeze-out effects at LT

**-130 °C ~ 140 K**

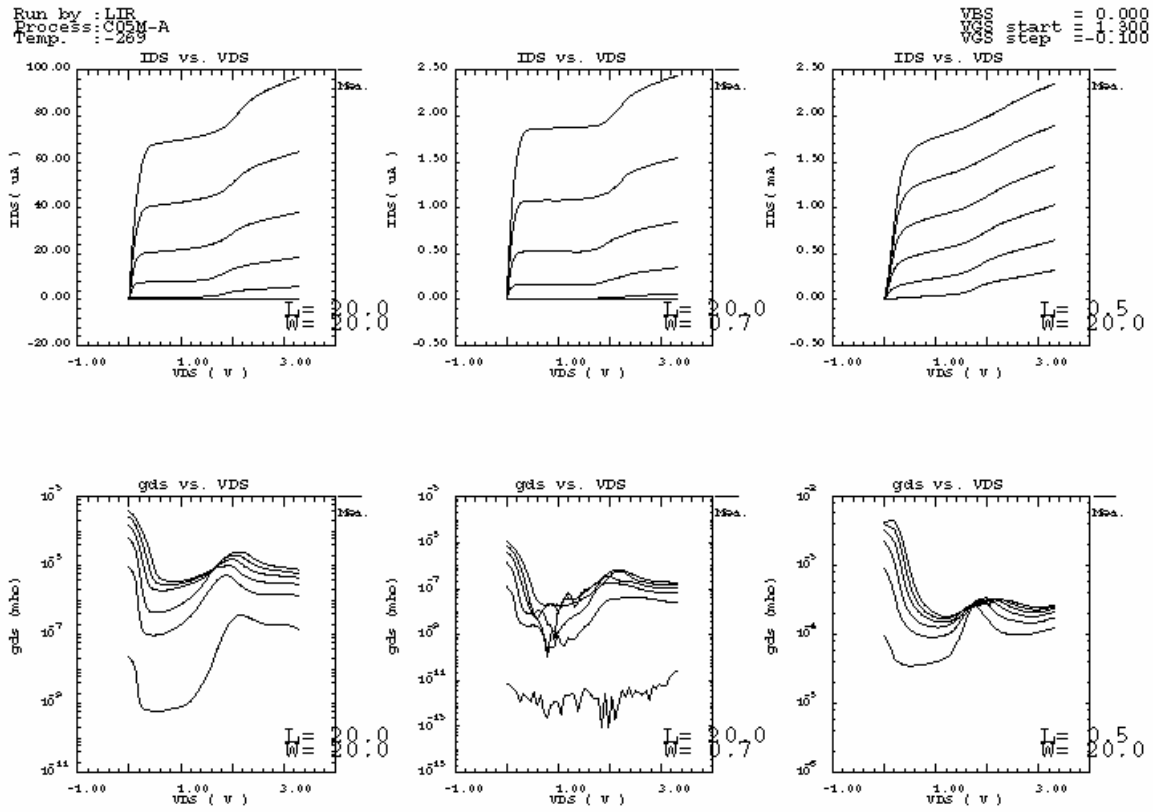
# Freeze-out effects at LT

1. Freeze-out effects in substrate ($T \leq 10$ K)

2. Freeze-out effects in buried channel PMOS

3. Freeze-out effects in LDD zones

# 1. Freeze-out effects at very LT



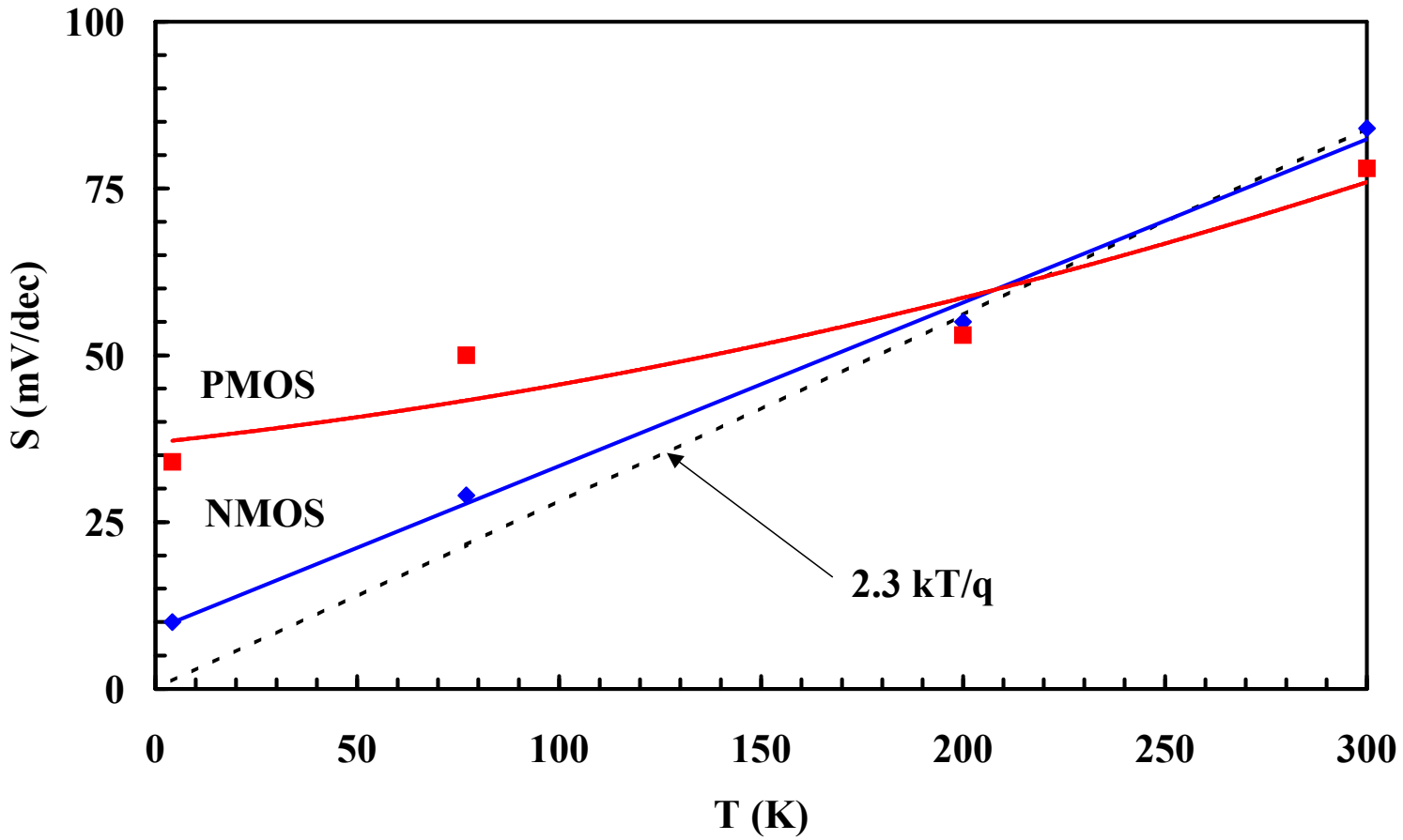

**Ids(Vds)**

**Gds(Vds)**

**T = 4.2 K ($L^4He$) : kink effect + hysteresis**

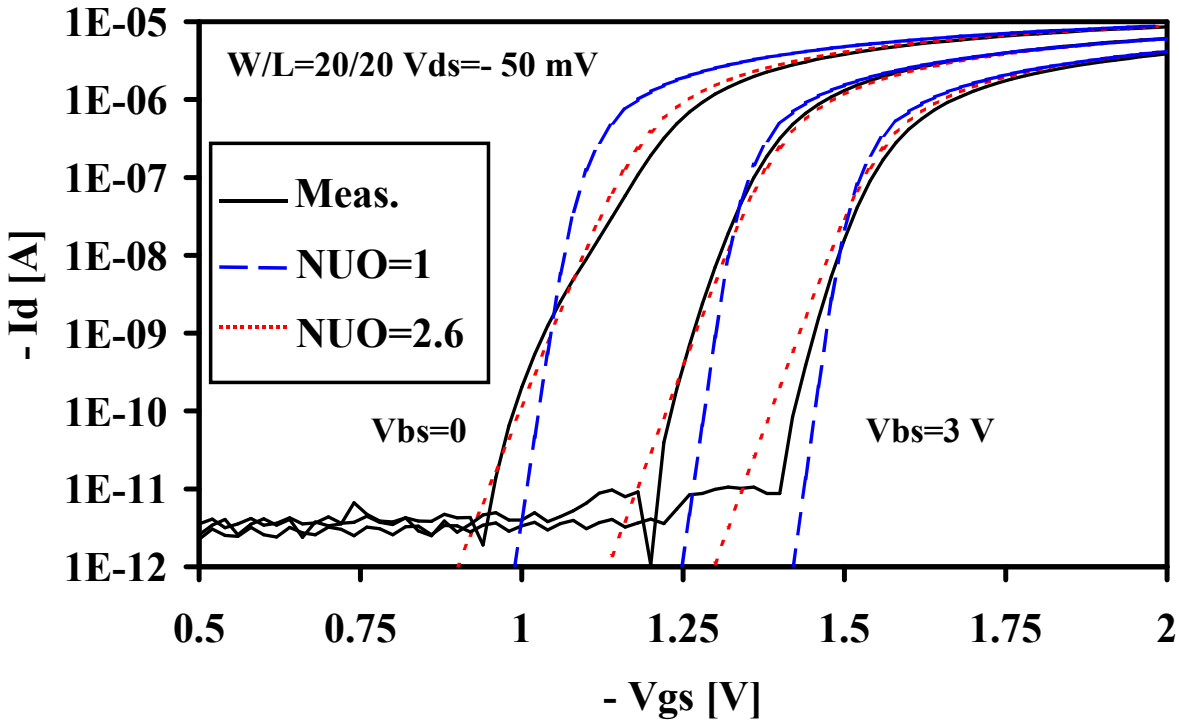
# 2. Freeze-out effects in buried channel PMOS

## Subthreshold swing in 0.5 µm CMOS with single $N^+$ poly-Si gate



# 2. Freeze-out effects in buried channel PMOS

## 0.35 µm CMOS with single $N^+$ poly-Si gate

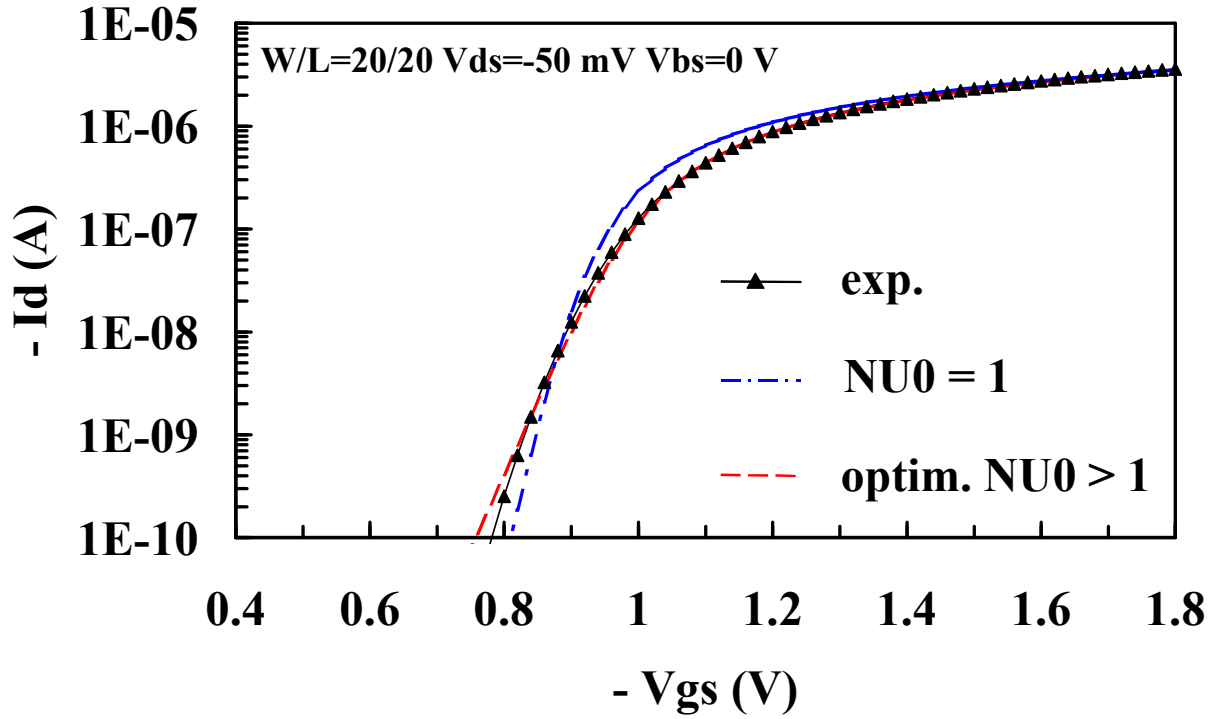



**T = 77 K**

- **Degradation of the weak inversion slope (T < 200 K)**
- **New parameter: NUO (1st-order estimation)**

# 2. Freeze-out effects in buried channel PMOS

## 0.21 µm CMOS with dual poly-Si gate: no buried channel



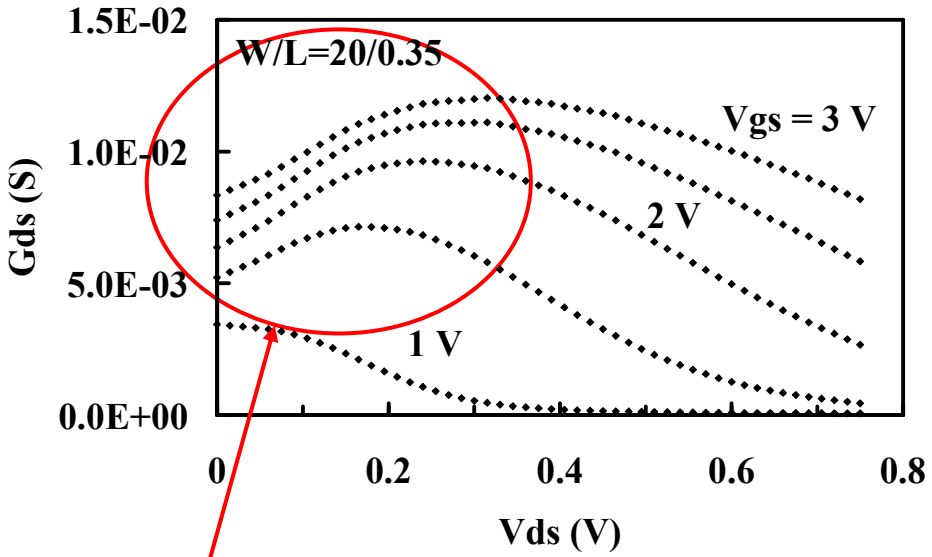

T = 77 K

- Less important degradation of the weak inversion slope
- Parameter NUO still needed: NUO=1.9 PMOS, NUO=1.5 NMOS

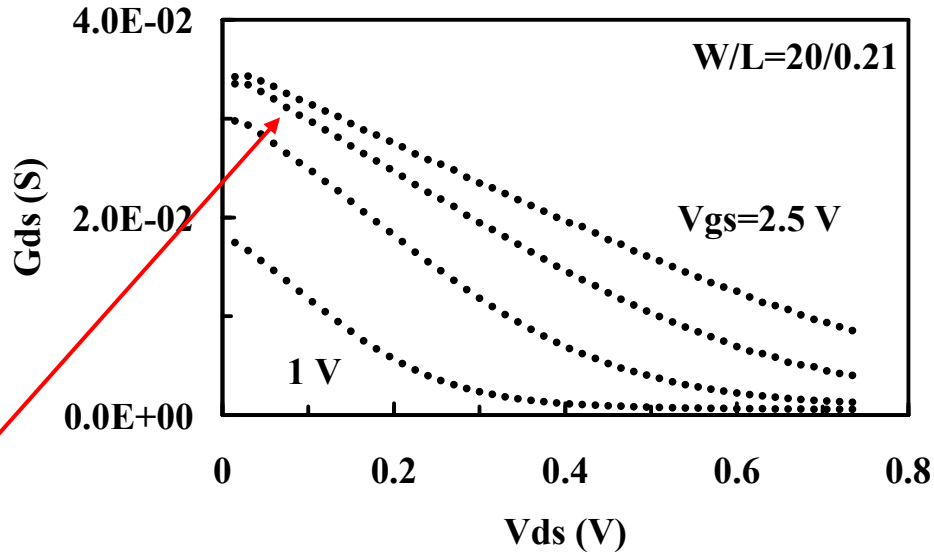
# 3. Freeze-out effects in LDD zones: NMOS 77 K

**Strong influence on Gds at T ≤ 150 K in prev. processes**

**0.35 µm CMOS process**




**0.21 µm CMOS process**




**Not modelised**

**No freeze-out effects in 0.21 µm tech.**
**Influence of pockets ?**

# Some examples of simulation

- **ELDO circuit simulator (Mentor Graphics)**

**+ UDM/CMPI (User Defined Model)**

- **UTMOST (Silvaco) for parameter extraction & optimization**

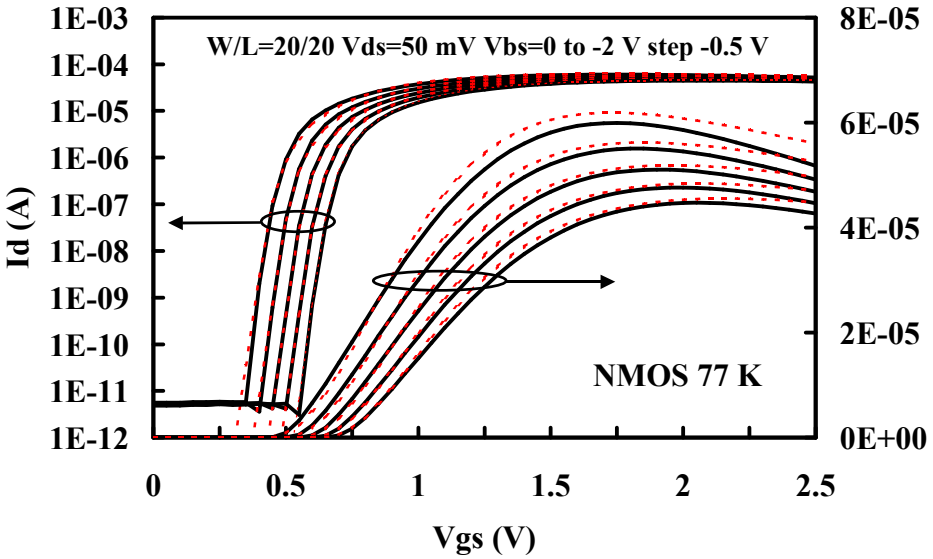
✓ **On 0.21 µm CMOS process**

✓ **After parameter optimisation: Lmin<L<20µm ; Wmin<W<20 µm ; weak/moderate/strong inversion**

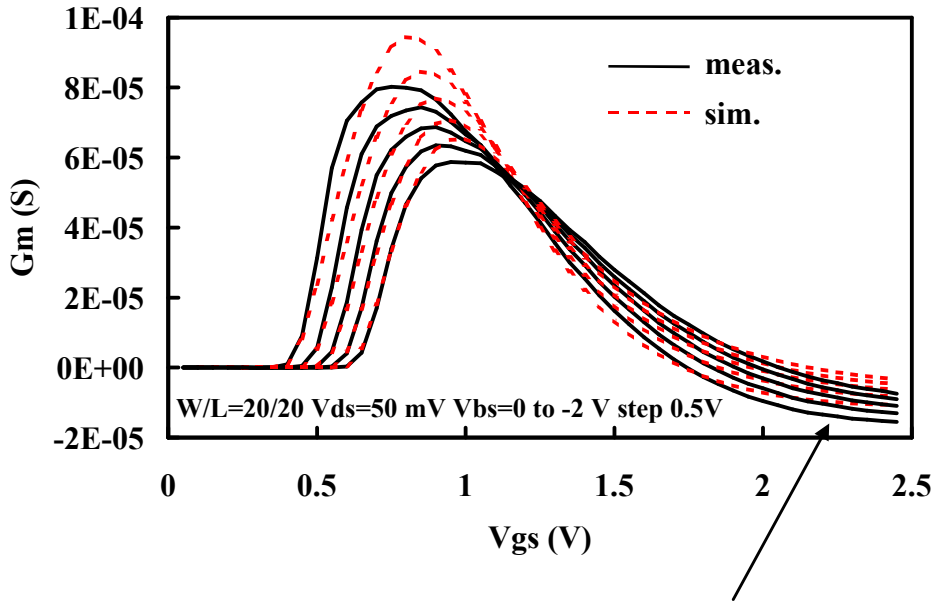
# Ex: NMOS transfer characteristics at 77 K (1/2)

***Linear (ohmic) regime Vds = 50 mV***

***Drain current Id***




***Gate transconductance Gm***

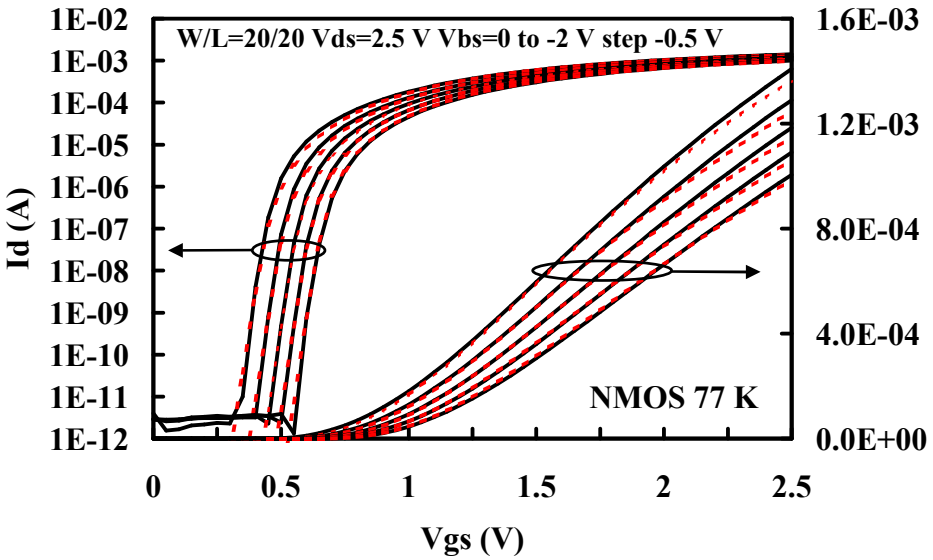



**Negative transconductance Gm**

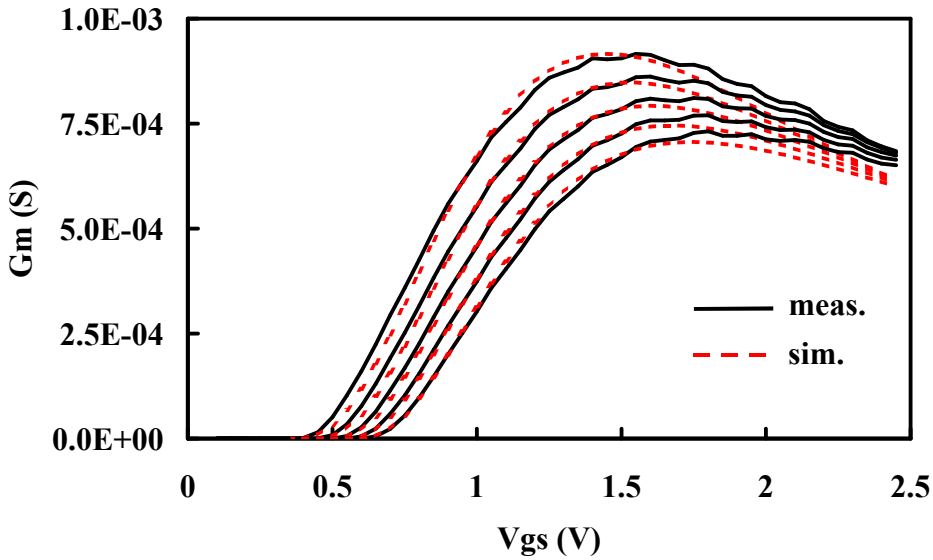
# Ex: NMOS transfer characteristics at 77 K (2/2)

***Saturation Vds = 2.5 V***

***Drain current Id***

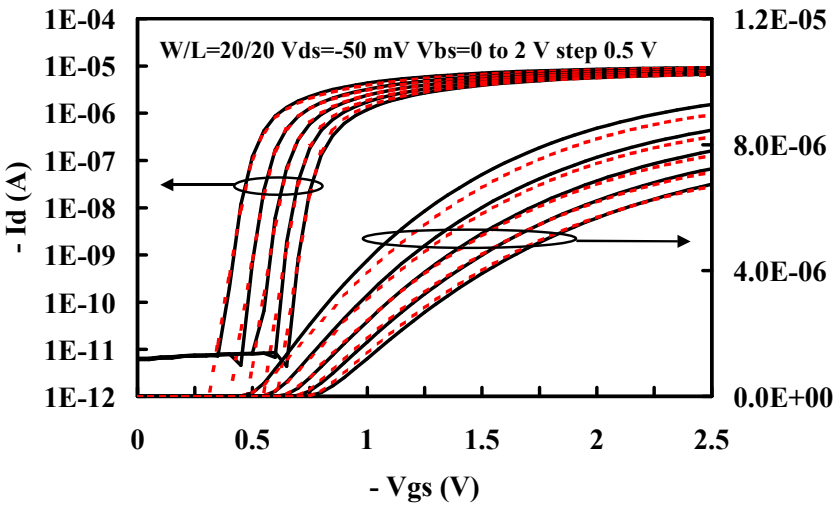


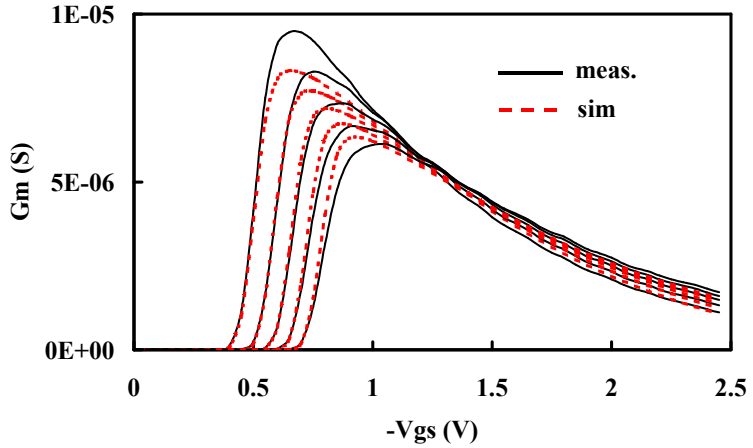

***Gate transconductance Gm***



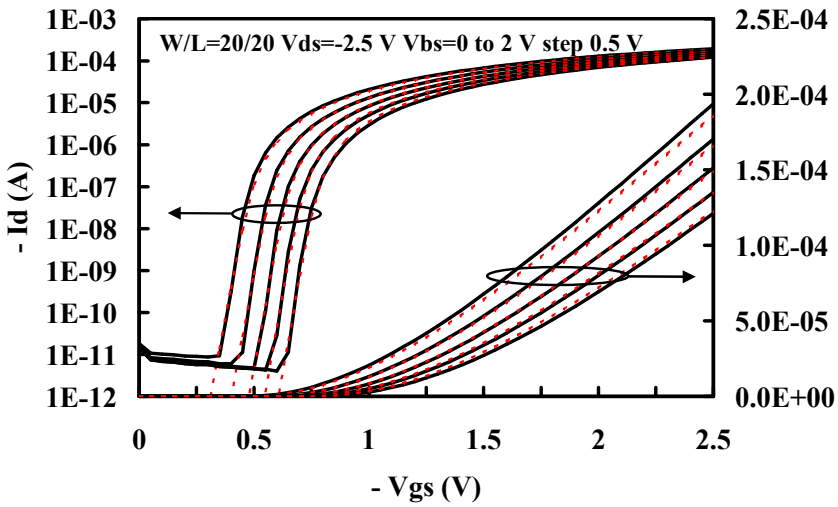
# Ex: PMOS transfer characteristics at 77 K

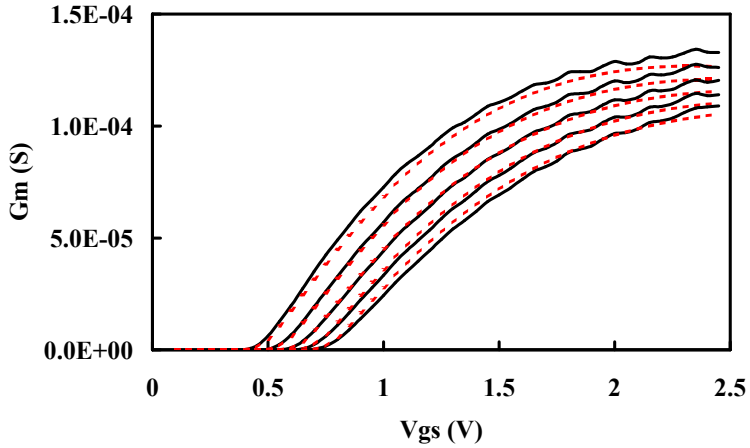
## *Linear regime Vds = - 50 mV*




## *Saturation Vds = - 2.5 V*

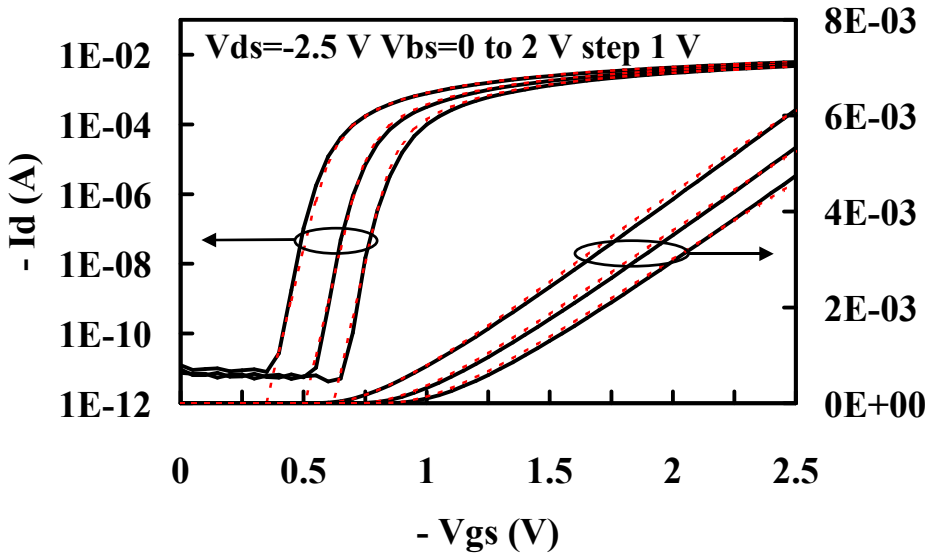


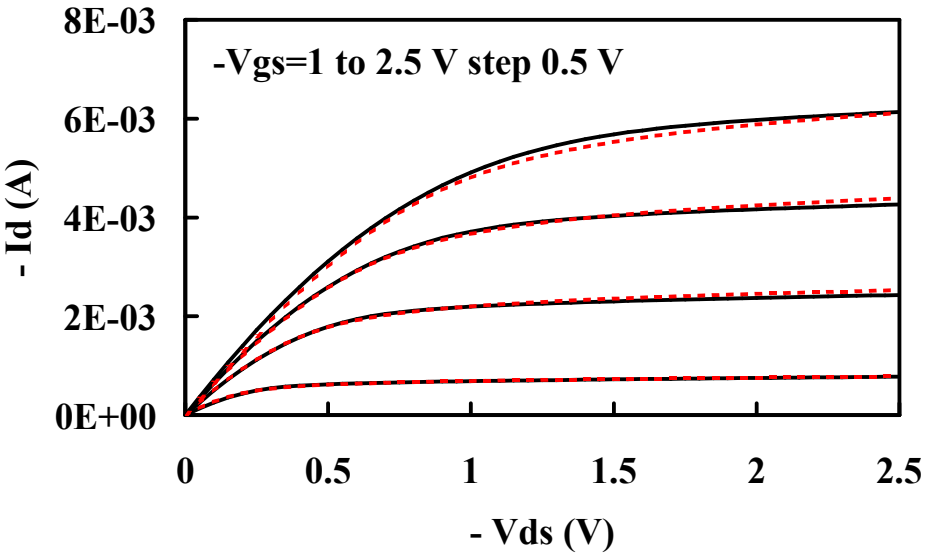
# Ex: Short-channel PMOS at 77 K

## W/L=20/0.32

### Id(Vg) Lin & Log

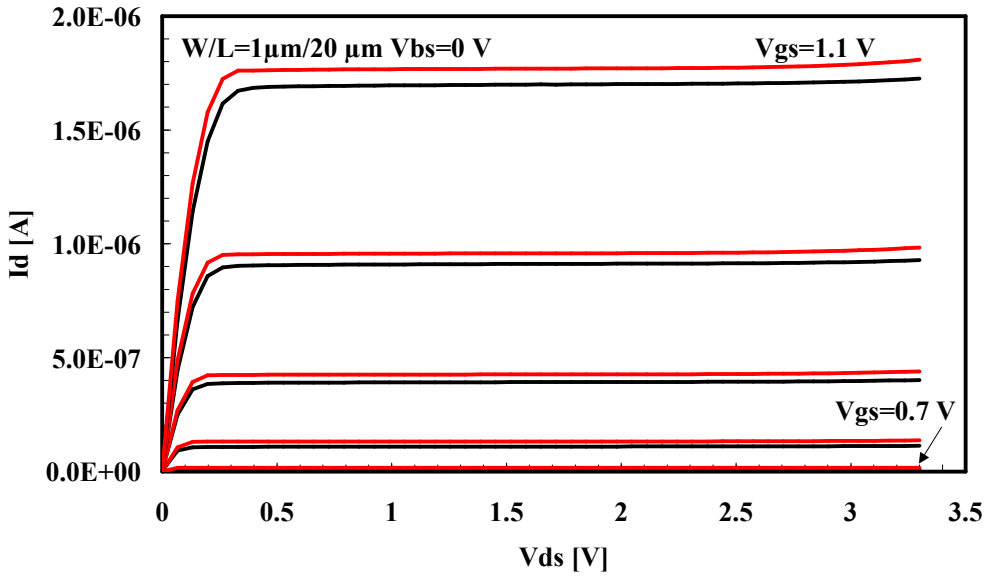



### Id(Vd)



# Ex: Long-channel NMOS 0.35 µm CMOS

***Drain current Id***

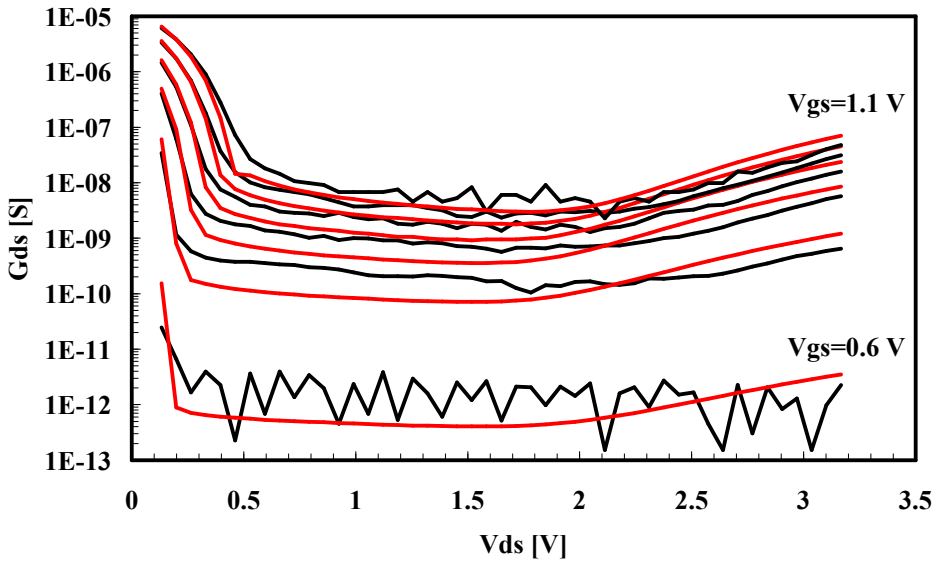



— exp

— sim

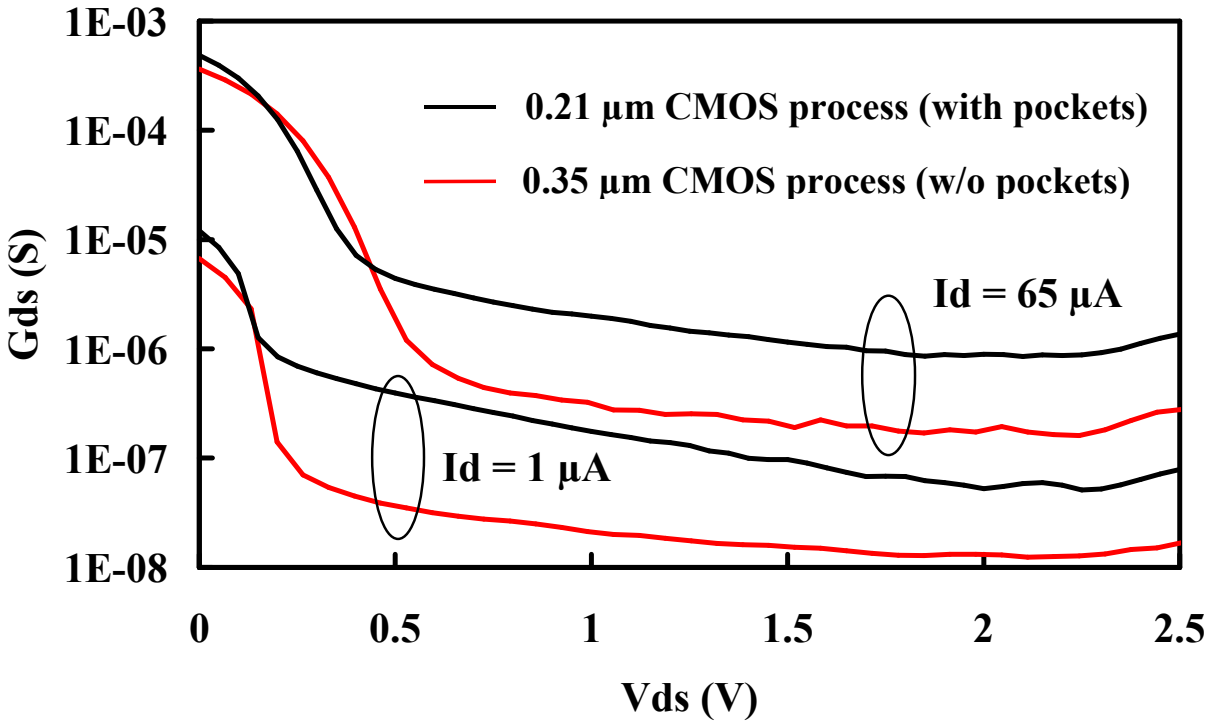
**NMOS output characteristics 77 K**

***Drain conductance Gds***



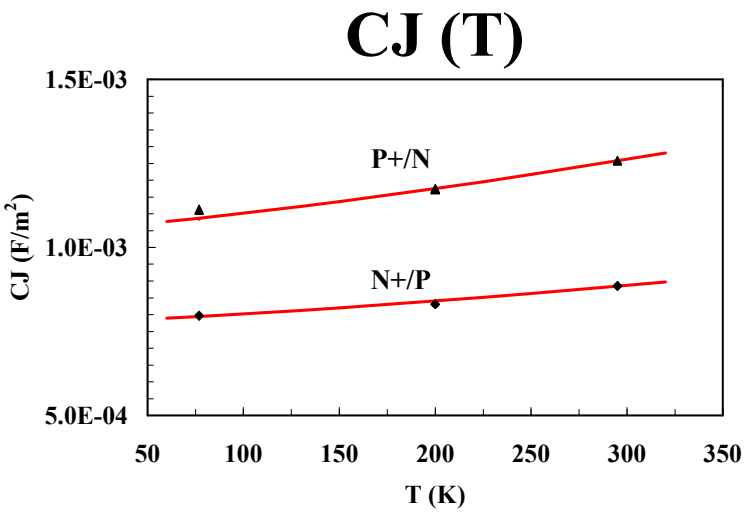
# Pocket implants & long channel MOSFETs

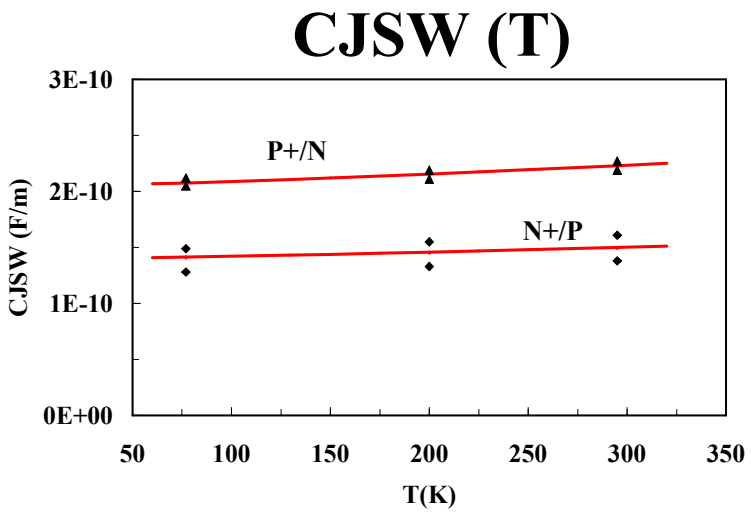
## NMOS drain conductance 77 K long-channel (L = 20 µm)

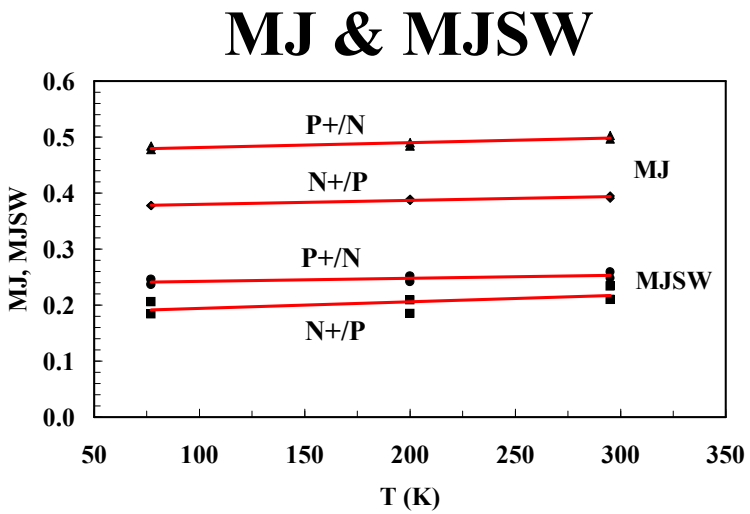



- Important degradation of Gds in saturation (≈ 1 decade)
- Effect not specific to LT; same problem at RT

# AC parameters vs. temperature



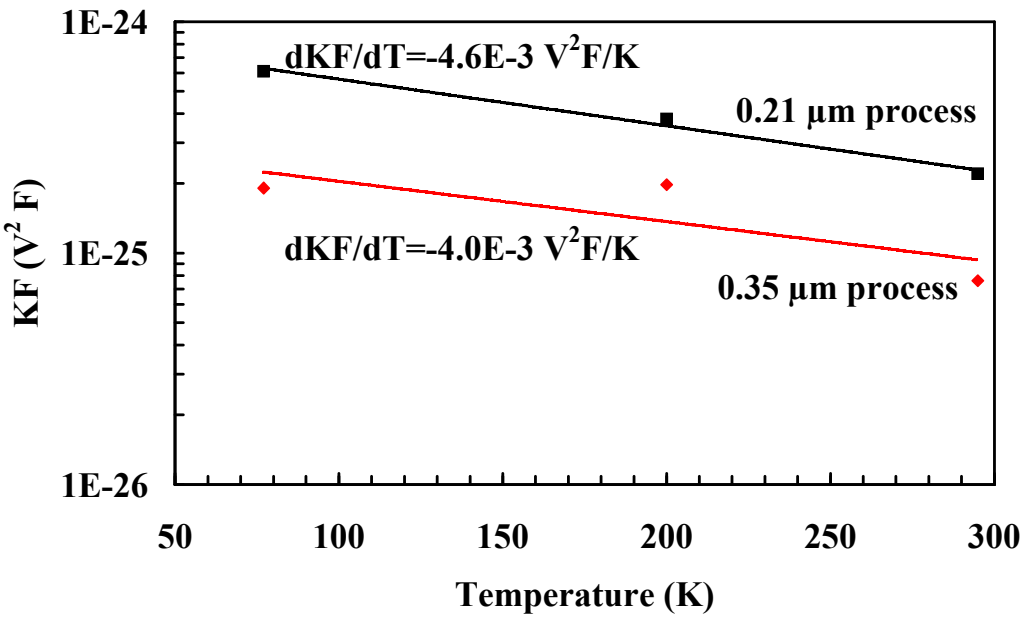



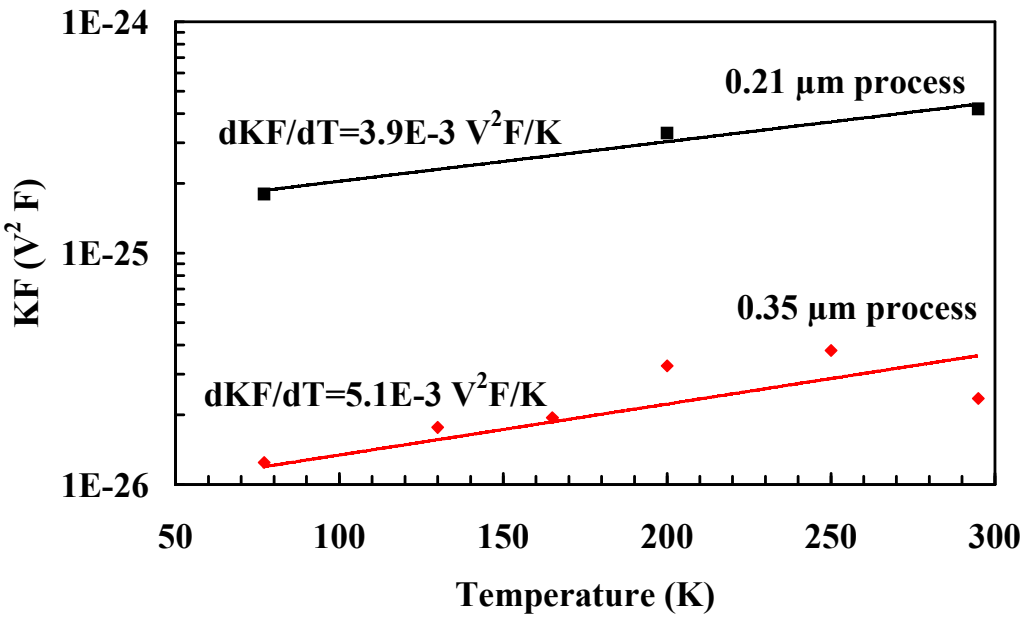
# Low frequency noise at LT

**1/f noise model in std. EKV 2.6 :**

$$S_{Id}\left(A^2/Hz\right)=\frac{KF\,G_m^2}{W\,L\,C_{ox}\,f^{AF}}$$

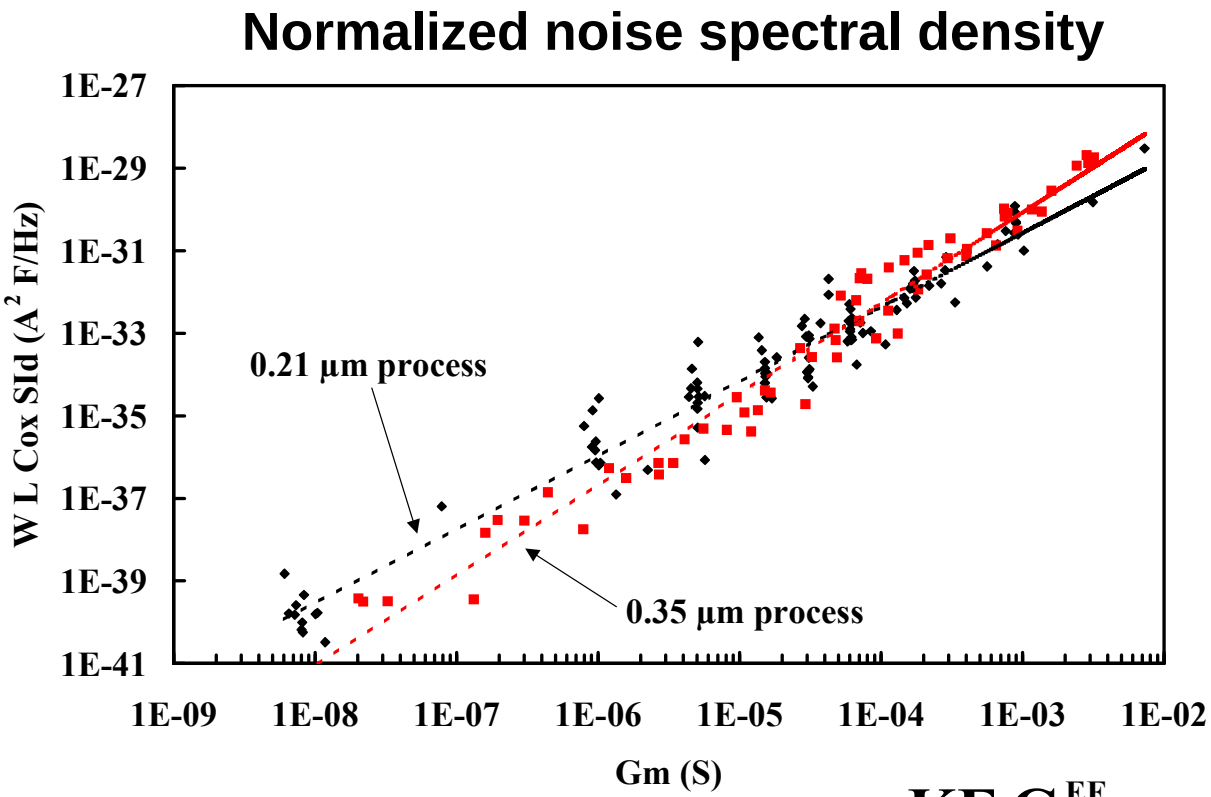
# LF noise and evolution with temperature




**After optimization in weak & moderate inversion**

# LFN model: test from weak to strong inversion

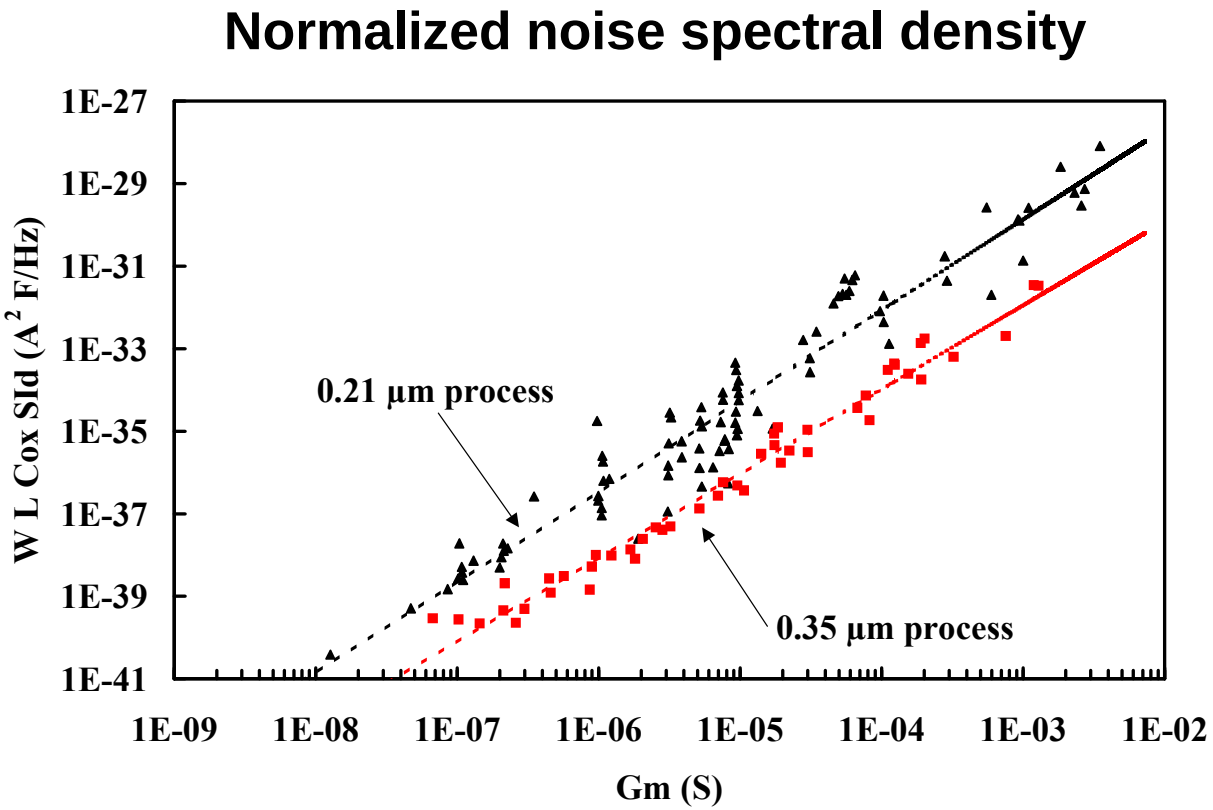



**NMOS T = 77 K**
**f = 1 Hz**
**|Vds| = 1.8 or 3.3 V**
**Wmin < W < 20 µm**
**Lmin < L < 20 µm**

- **Better agreement:** $S_{Id} = \frac{KF\, G_m^{EF}}{W\, L\, C_{ox}\, f^{AF}}$

- **For 0.5, 0.35 & 0.21 µm CMOS, single & dual gate processes, RT & LT: 1.8 < EF < 2.3 (tech. dependent)**

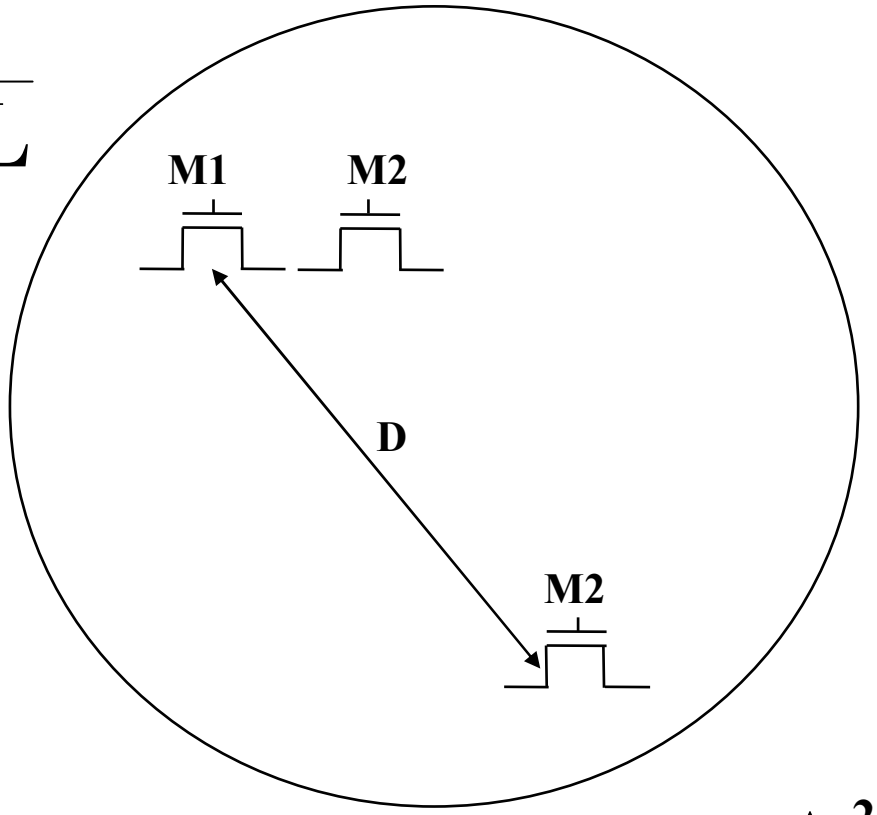
# LFN model: test from weak to strong inversion




**PMOS T = 77 K**
**f = 1 Hz**
**|Vds| = 1.8 or 3.3 V**
**Wmin < W < 20 µm**
**Lmin < L < 20 µm**

# MOSFET matching at low temperature

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL}$$




**Pelgrom model (1989)**

**(P = VTO, β, γ)**

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2$$

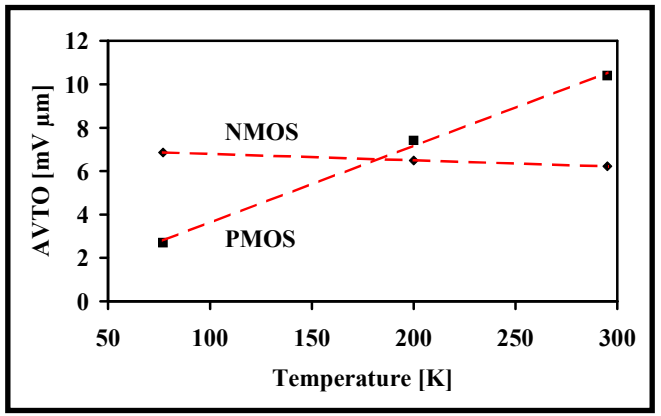
# Transistor matching: parameter extraction

- NMOS & PMOS modules (21 transistors ; 6 different sizes : WxL = 12.6x12.6, … 0.5x0.35 µm² ; D = 14 µm)
- P = VTO (threshold voltage), KP (current factor), GAMMA (substrate coefficient)
- Extracted parameters: AVTO, AKP, AGAMMA
- Measurements in linear regime at RT, 200 K & 77 K
- Matching data at LT: very scarce in literature

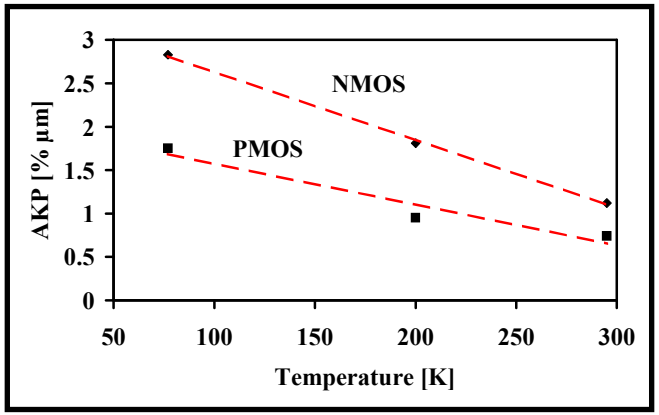
# Transistor matching: results on a 0.35 µm CMOS process with single $N^+$ poly-Si gate

**Tox = 7.5 nm**

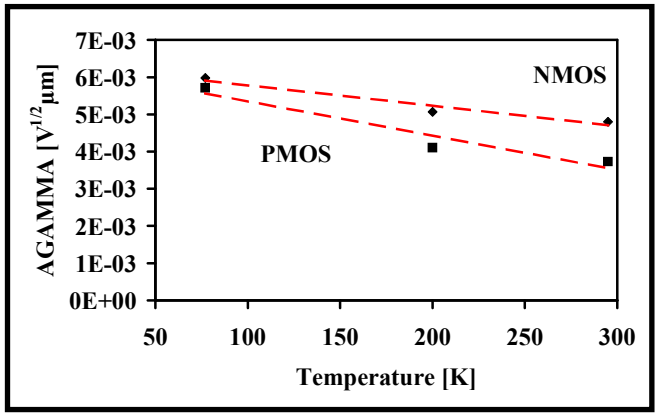
## *Threshold voltage*




## *Current factor*



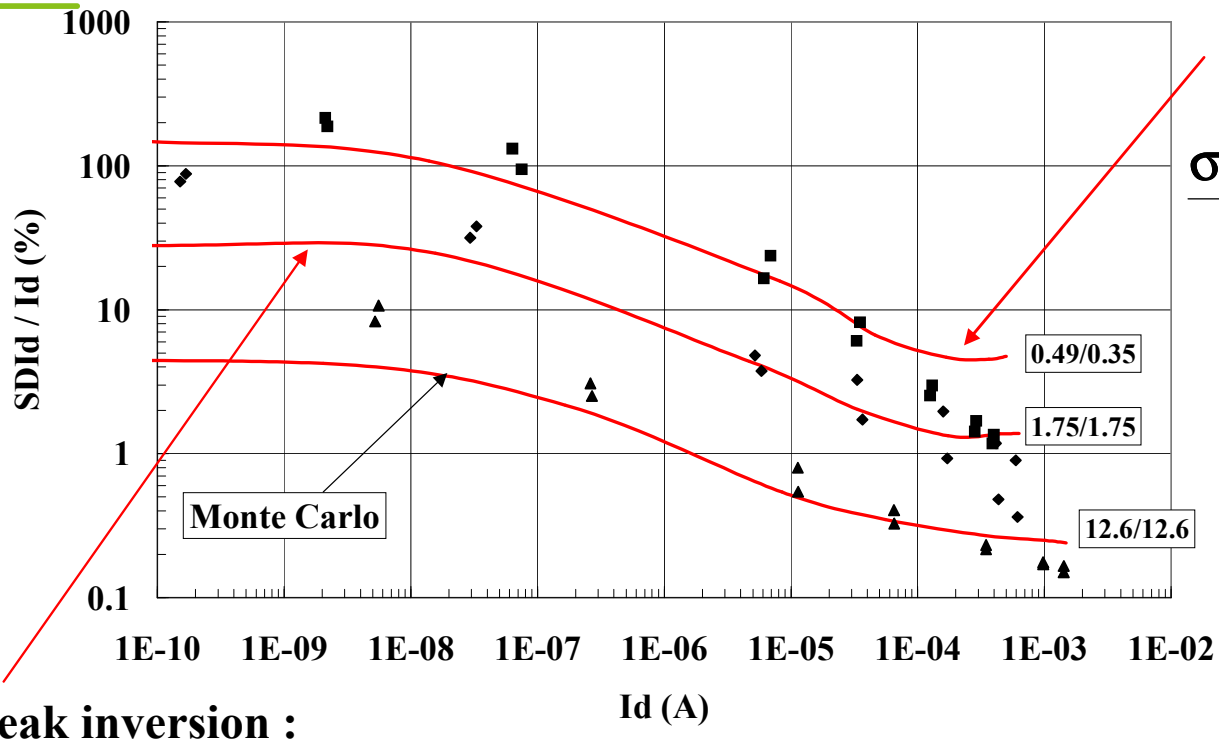

## *Substrate coeff.*



# Transistor matching: results

- **In general, poorer matching at LT**
- **Notable exception : threshold voltage of PMOS with buried channel ; AVTO extremely small at 77 K (same behavior on PMOS 0.7 µm $N^+$ gate process)**

# MOSFET matching parameters: verification in saturation




**Strong inversion :**

$$\frac{\sigma(\Delta I_d)}{I_d} = \sqrt{\frac{\sigma^2(\Delta\beta)}{\beta^2} + 4\,\frac{\sigma^2(\Delta VTO)}{(V_{GS} - V_{th})^2}}$$

**Weak inversion :**

$$\frac{\sigma(\Delta I_d)}{I_d} = \frac{1}{n\,V_t}\,\sigma(\Delta VTO)$$

**NMOS 77 K Vds=3.3 V Vbs=0 V**

# MOSFET matching parameters: implementation in ELDO ?

## EKV 2.6 Model Equations:

### 5.5 Short distance matching

Random mismatch between two transistors with identical layout and close to each other is in most cases suitably described by a law following the inverse of the square root of the transistors' area. The following relationships have been adopted:

$$\mathrm{VTO}_a = \mathrm{VTO} + \frac{\mathrm{AVTO}}{\sqrt{\mathrm{NP} \cdot W_{eff} \cdot \mathrm{NS} \cdot L_{eff}}} \quad (27)$$

$$\mathrm{KP}_a = \mathrm{KP} \cdot \left(1 + \frac{\mathrm{AKP}}{\sqrt{\mathrm{NP} \cdot W_{eff} \cdot \mathrm{NS} \cdot L_{eff}}}\right) \quad (28)$$

$$\mathrm{GAMMA}_a = \mathrm{GAMMA} + \frac{\mathrm{AGAMMA}}{\sqrt{\mathrm{NP} \cdot W_{eff} \cdot \mathrm{NS} \cdot L_{eff}}} \quad (29)$$

These model equations are only applicable in Monte-Carlo and sensitivity simulations.

NOTE: since negative values for both $\mathrm{KP}_a$ and $\mathrm{GAMMA}_a$ are not physically meaningful, these are clipped at zero.

# Summary and conclusion

- Specific model based on std. EKV 2.6
- 2 main improvements: mobility, weak inv. slope degrad.
- Only 6 additional parameters
- 0.7 - 0.5 - 0.35 and 0.21 µm CMOS std. bulk processes
- EKV-LT model implemented in ELDO and UTMOST
- Still compact and continuous charge-based model
- Additional results on LF noise and transistor matching evolution with temperature
- Excellent tool for analog IC design at LT

# References


[1] F. Théodoloz, C. Enz, M. Bucher, Charge Based MOS Transistor Mobility Modelling Applicable at Low Temperature, unpublished EPFL Technical Report

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