Comparison of 0.35 and 0.21 µm CMOS Technologies for Low Temperature Operation (77 K – 200 K) and Analog Circuit Design

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INTRODUCTION

This paper deals with the simulation of hybrid CMOS readout circuits working at low or at intermediate temperature, typically 77 K, 130 K or 200 K, such as those used in high performance infrared image sensors. SPICE parameters of transistors, including DC, AC, 1/f noise and matching parameters, are mandatory for design and simulation of such circuits. However CMOS foundries do not provide full sets of MOSFET parameters for simulation at temperature lower than -55°C (≈ 220 K). So these MOSFET parameters must be extracted prior to circuit simulation. Furthermore the used MOSFET model must address the important weak and moderate inversion regimes where most of the transistors of the CMOS readout circuits are operating. In this work we use a specific model based on the EKV 2.6 compact charge model formalism [1]. This model was previously described and applied to different CMOS bulk processes such as 0.7 µm / 5 V [2], 0.5 - 0.35 µm / 3.3 V [3] and 0.21 µm / 1.8 V [4] from different foundries optimized for room temperature operation. The model's performance is described in this paper for two commercial processes from the same foundry, namely a 0.35 µm / 3.3 V and a 0.21 µm / 1.8 V CMOS technology. As noise is a key concern in analog circuits, experimental results on the low frequency noise parameters for both NMOS and PMOS transistors at low temperature from these two processes are also presented.

CMOS PROCESSES

We characterize two CMOS processes from the same foundry (Atmel). The first process is a 0.35 µm process with a single N^+ polysilicon gate operating at 3.3 V (Tox = 7.5 nm). The threshold voltage temperature coefficients (TCV) for n-MOSFETs and p-MOSFETs are different: + 0.71 mV/K for NMOS and -1.58 mV/K for PMOS. NMOS transistors are surface channel transistors. PMOS are buried-channel PMOS and an unusual behavior is observed at temperature lower than 200 K in the subthreshold region of the transfer characteristics Id (Vgs) of such transistors. The second process is a 0.21 µm process operating at 1.8 V (Tox = 3.9 nm). This process uses two kinds of polysilicon gates, N^+ doped polysilicon gate for NMOS and P^+ doped polysilicon gate for PMOS (dual gate process). As a consequence both NMOS and PMOS are surface channel transistors and the threshold voltage temperature coefficients are nearly equal, + 0.53 mV/K for n-MOSFETs and - 0.67 mV/K for p-MOSFETs. This deep submicron process offers also a thicker oxide for operation at higher voltage (3.3 V), which however will not be discussed in this paper, and has pocket implants to combat short channel effects. Finally we have to mention that both processes have LDD zones and that NMOS present a reverse short-channel (RSCE) effect. PMOS transistors of the 0.21 µm process also present a RSCE effect. We observe a significant reduction of this RSCE effect with temperature as described in [5].

THE EKV 2.6 MODEL AT LOW TEMPERATURE

Description

The standard EKV 2.6 model [1] from EPFL was initially built to operate in usual temperature ranges, typically from -55 to +125 °C. For temperatures typically below 200 K, a modified model has to be used due to physical phenomena specific to low temperature. In particular this model incorporates a charge-based mobility model for low temperature

application including Coulomb, phonon and surface roughness scattering mechanisms as well as velocity saturation [6]. The mobility law for the effective vertical field is given by:

$$\mu = \frac{\mu_0}{\left(\frac{E_{eff}}{ECO}\right)^{\alpha_1} + \left(\frac{E_{eff}}{EPH}\right)^{1/3} + \left(\frac{E_{eff}}{ESR}\right)^2} \quad (1)$$

where ECO, EPH, ESR, α_1 and μ_0 are adjustable parameters, and E_{eff} the vertical electrical field in the inversion layer, which is a function of the inversion charge Q_i and of the bulk charge Q_b:

$$E_{eff} = \frac{q\,(\eta\, Q_i + Q_b)}{\varepsilon_{Si}} \quad (2)$$

with η = 1/2 for NMOS and 1/3 for PMOS.

The relationship among charges and applied biases is provided by the charge-voltage relationship provided by the EKV model valid at all levels of inversion. The vertical field mobility model is also combined with a charge-based expression for the effect of velocity saturation, extending the application to short-channel as well, where the critical field UCRIT is a (temperature dependent) model parameter. Unlike common MOSFET models, the present model accounts for position- (and bias-) dependence of mobility through the MOS channel. The mobility model is therefore fully consistent with the basic charge model approach. The resulting compact model is overall very coherent as well as continuous in all operating regions, from weak to strong inversion and from triode to saturation. Further specific features, such as improved accounting for weak inversion slope degradation, completed the present specific low-temperature extensions of the EKV model.

The full model was implemented in the ELDO® circuit simulator from Mentor Graphics as a proprietary model using the User Defined Model (UDM/CMPI) interface. It was also implemented in the Silvaco UTMOST® software used for device parameters extraction and optimization.

Application of the LT EKV 2.6 Model

The improved charge-based mobility model allows to reproduce accurately the drain current as seen in Fig. 1 for NMOS transistors of the 0.21 µm technology. It allows also to reproduce accurately the gate transconductance (Gm) which could be even negative on NMOS transistors in the ohmic mode at high vertical fields (Fig. 2). The simulated characteristics in these figures were obtained after optimization on different MOSFETs with drawn length down to 0.21 µm and drawn width down to 0.6 µm.

For p-MOSFETs of the 0.35 µm process, the weak inversion slope no longer decreases at temperature lower than 200 K. This freeze-out effect in the buried channel is taken into account as a first approximation in this compact model by introducing an effect degrading the weak inversion slope with respect to its theoretical value. An empirical parameter NU0 is introduced, having an ideal value of NU0 ≡ 1, corresponding to the absence of interface states. This parameter allows minimizing the error in weak inversion as illustrated in Fig. 3, but does not affect the strong inversion regime. For the PMOS transistors we measure NU0 = 2.6 while for the NMOS transistors we obtain NU0 = 1.3. Although PMOS transistors of the 0.21 µm process do not experience any buried channel freeze-out effect, the optimized value of the NU0 parameter was higher than unity at 77 K (NU0 = 1.9). For NMOS transistors the optimized value was NU0 = 1.5.

The mobility in short-channel transistors, particularly for NMOS, is strongly affected by velocity saturation of the carriers, limiting the total available drain current. Figure 4 shows the evolution of the saturation drain current at 77 K relative to its value at 293 K for NMOS and PMOS devices with channel length. While for the 0.35 µm process this ratio is 3.4 and 2.6 at long channel, it drops to 1.4 and 1.2 at short channel, for NMOS and PMOS transistors, respectively. For the 0.21 µm process this ratio is 3 and 1.9 at long channel, it also drops to 1.4 and 1.2 at short channel, for NMOS and PMOS transistors, respectively. This indirectly illustrates the importance of velocity saturation which remains one of the main effects limiting short-channel device performance at low temperature.

As the 0.21 µm deep submicron CMOS technology has pocket implants, we observe an important increase of the drain conductance (Gds) in saturation on long channel transistors [7, 8]. This effect is not yet modeled in the framework of the EKV 2.6 model and it was necessary to extract two sets of parameters, a first one for drawn length covering 0.21 and 0.5 µm and a second one for greater length. In contrast, this procedure was unnecessary for the 0.35 µm process.

A carrier freeze-out effect is observed in the LDD zones of the 0.35 µm CMOS process at temperatures lower than 150 K. This phenomenon leads to an important error when evaluating the drain conductance of short transistors at very low drain-to-source voltages (less than 250 mV) in strong inversion (Fig. 5). Although LDD zones also exist in the present 0.21 µm process, we do not observe any freeze-out effects down to 77 K. This is probably due to the existence of highly doped pockets in this technology.

LOW FREQUENCY NOISE PARAMETERS

Flicker noise parameters were extracted on these technologies using the following model implemented in the standard EKV model:

$$S_{Id} = \frac{KF\, G_m^2}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \tag{3}$$

For analog application, special emphasis was placed on extracting the noise parameters in the weak and moderate inversion regimes. Noise measurements were done in saturation (|Vds| = 1.8 V or 3.3 V) on different devices with length varying between L_{min} and 20 µm and width between 1 and 20 µm. Noise spectral densities measured at different gate transconductance (Gm) were then optimized. The evolution of the flicker noise parameter KF with temperature obtained after optimization in weak-moderate inversion is shown in Fig. 6 and 7 for NMOS and PMOS respectively. For NMOS transistors we observe an increase of the KF parameter at low temperature. We also observe that the LF noise increases on the more advanced process. This is probably due the nitrided gate oxide used in advanced sub-0.25 µm CMOS processes [9]. Contrary to NMOS transistors, the KF parameter of PMOS transistors decreases with temperature, whether the channel is buried or not. We observe a significant increase of noise in the 0.21 µm CMOS process for this type of transistor.

The preceding flicker noise model was also tested at room temperature and at 77 K in a wider range of gate transconductance covering also the strong inversion regime (Fig. 8 and 9). We experimentally found that a better agreement with measurements would be obtained by modifying (3) according to:

$$S_{Id} = \frac{KF\, G_m^{EF}}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \tag{4}$$

where EF is a process-dependent exponent, not strictly equal to 2, allowing to reproduce the bias dependence ([10] and references therein) of input referred noise voltage S_{Id} / Gm^2. The EF parameter values we measure for NMOS and PMOS transistors from different 0.5, 0.35 and 0.21 µm technologies at low temperature or at room temperature lie between 1.8 and 2.3.

SUMMARY

A comparison has been made at low temperature on MOSFETs in 0.35 µm and 0.21 µm technologies. Important differences are seen on these processes when cooling the transistors at 77 K. These differences affect both the DC characteristics and 1/f noise.

Experimental results on the evolution of the low-frequency noise parameters at low temperature down to 77 K for both NMOS and PMOS transistors have been presented. For PMOS transistors, a decrease of the KF parameter – independently whether a buried channel is used or not – could be found experimentally when lowering the temperature, contrary to the increase found in NMOS transistors.

A specific model based on the EKV 2.6 compact MOSFET model was successfully applied for parameter extraction and simulation at low temperature of analog circuits. An evolved mobility model and an improved accounting for weak

inversion slope degradation allow this model to be successfully applied in all inversion regimes and over different geometries and temperatures on different technologies.

ACKNOWLEDGEMENTS

This work was supported by Commissariat à l'Énergie Atomique (CEA) and the French Ministry of Defense (DGA-STTC).

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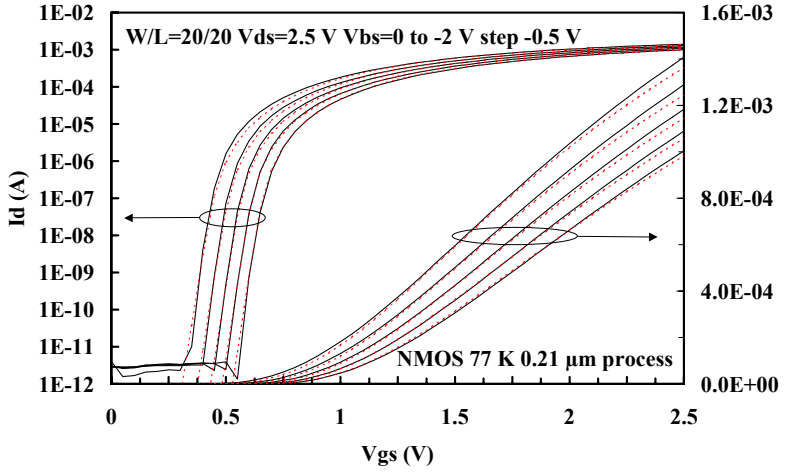

Fig. 1 Measured (–) and simulated (…) NMOS drain current with the EKV/LT model at 77 K in saturation

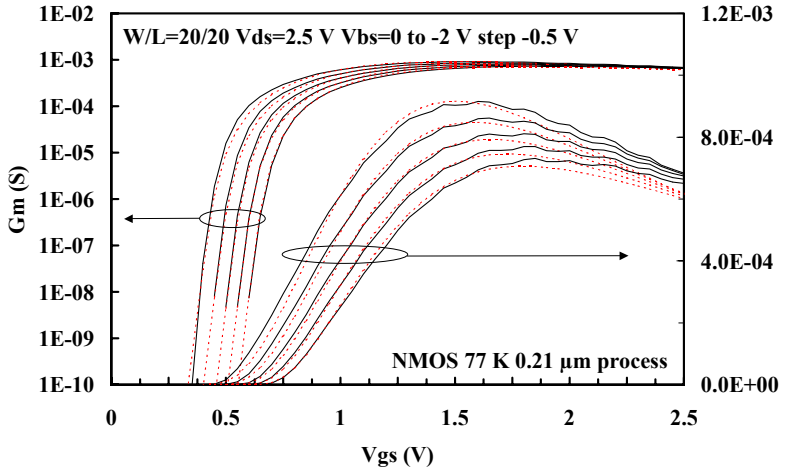

Fig. 2 Measured (–) and simulated (…) NMOS gate transconductance at 77 K

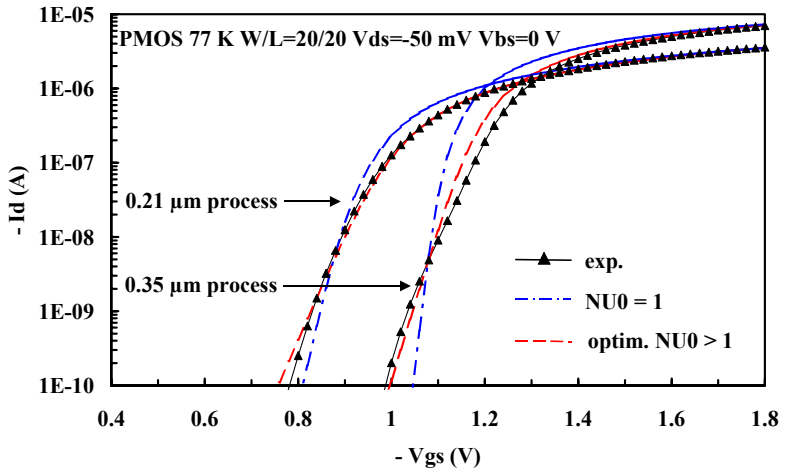

Fig. 3 PMOS transfer characteristics from the two technologies at 77 K

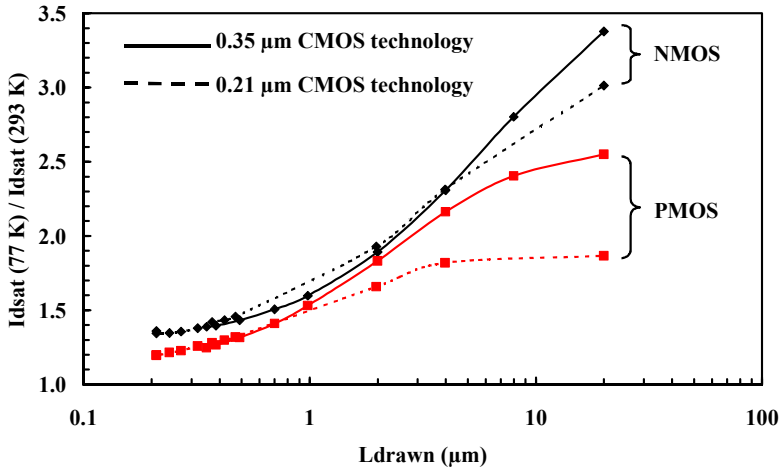

Fig. 4 Ratio of saturation drain current at 77 K and 293 K for NMOS and PMOS transistors from the two CMOS processes

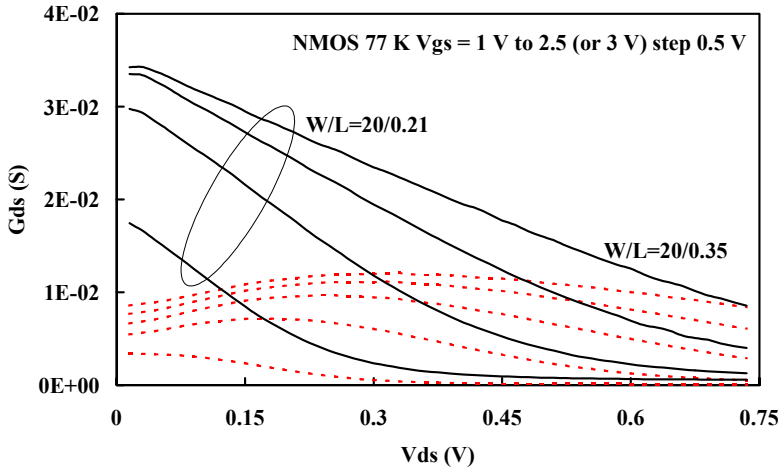

Fig. 5 Carrier freeze-out effects in NMOS transistors at 77 K in the 0.35 µm and 0.21 µm processes

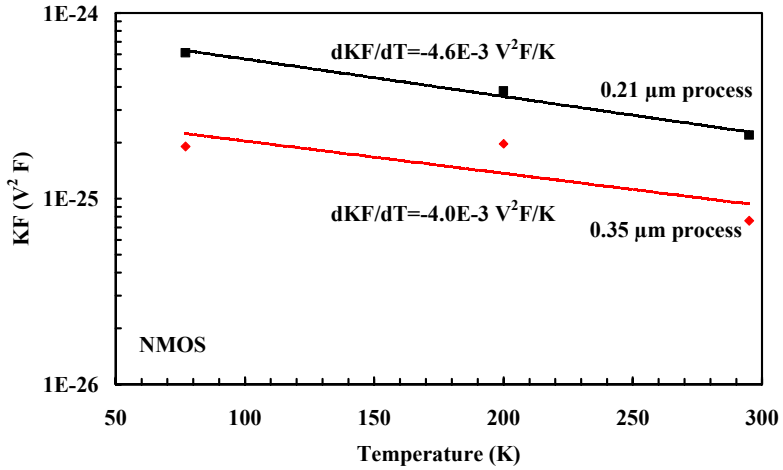

Fig. 6 Evolution of the flicker noise parameter KF with temperature for NMOS transistors for the two technologies

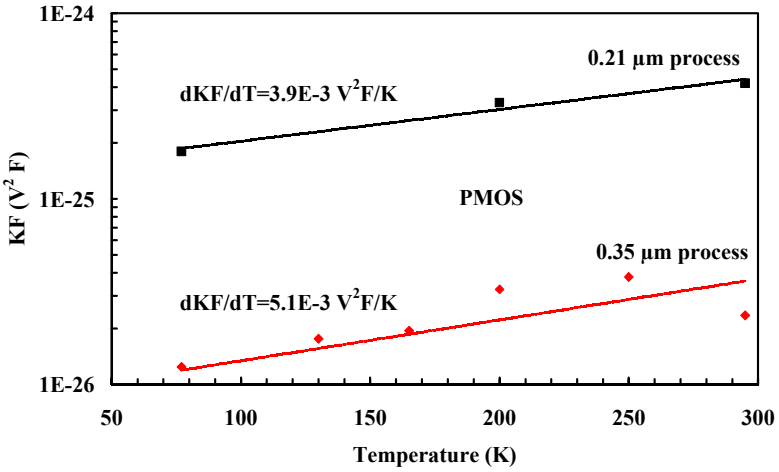

Fig. 7 Evolution of the flicker noise parameter KF with temperature for PMOS transistors

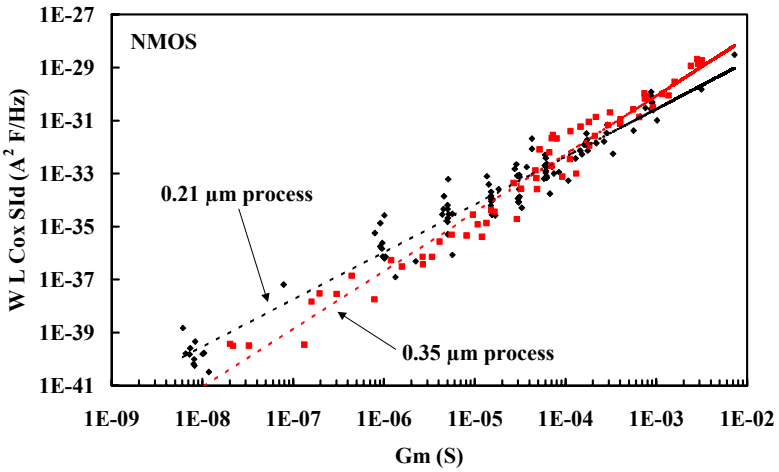

Fig. 8 Test of the flicker noise model at 77 K for NMOS transistors

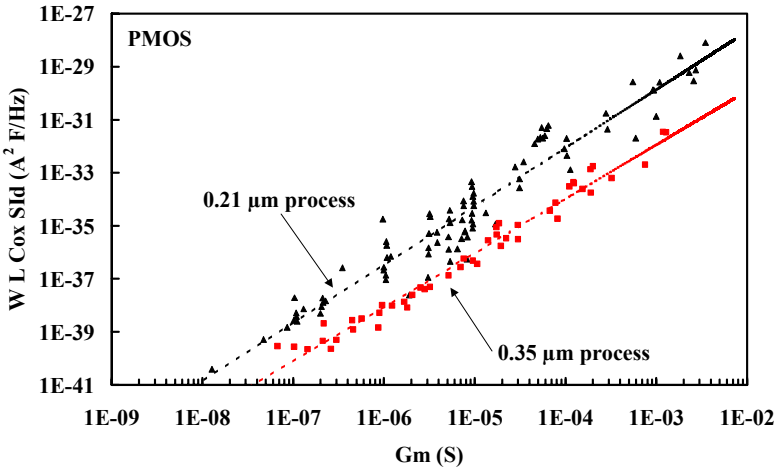

Fig. 9 Test of the flicker noise model at 77 K for PMOS transistors