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MOSFET MODELING FOR LOW TEMPERATURE (77 K – 200 K) ANALOG CIRCUIT DESIGN

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ABSTRACT: A compact MOSFET model based on the standard EKV 2.6 model is used for analog circuit simulation at low temperature. Device performance at 77 K is studied in this paper for a 0.21 µm CMOS technology with dual polysilicon gate and pocket implants, and conclusions are drawn for the applicability of the low-temperature version of the EKV MOSFET model.

INTRODUCTION

SPICE parameters are needed for simulation of CMOS readout circuits used in infrared image sensors working at low temperature, typically between 77 K and 200 K. Since foundries do not provide them, full sets of MOSFET parameters (DC, AC, 1/f noise parameters and matching parameters) must be extracted using a MOSFET model especially addressing the important weak and moderate inversion regimes where most of the transistors of the CMOS readout circuits are operating. In this paper we use a specific model based on the EKV 2.6 compact charge model formalism [1]. It was successively applied to different CMOS bulk processes such as 0.7 µm-5 V [2], 0.5 and 0.35 µm-3.3 V [3], with and without dual polysilicon gates, from different foundries. The model's performance at 77 K is evaluated in this paper for a more advanced process, namely a 0.21 µm-1.8 V dual gate oxide/dual polysilicon CMOS technology from Atmel. Experimental results on the low frequency noise parameters for both NMOS and PMOS transistors are also presented.

THE LOW TEMPERATURE VERSION OF THE EKV 2.6 MODEL

The standard EKV 2.6 model [1] from EPFL was initially built to operate in usual temperature ranges, typically from –40 to 120 °C. For temperatures typically below 200 K, the EKV 2.6 model is however unable to reproduce experimental electrical characteristics accurately enough. A modified model has then to be used due to physical phenomena specific to low temperature. In particular this model incorporates a new charge-based mobility model for low temperature application including Coulomb, phonon and surface roughness scattering mechanisms as well as velocity saturation [4]. The mobility law for the effective vertical field is given by:

$$\mu = \frac{\mu_0}{\left(\frac{E_{eff}}{ECO}\right)^{\alpha_1} + \left(\frac{E_{eff}}{EPH}\right)^{1/3} + \left(\frac{E_{eff}}{ESR}\right)^{2}} \quad (1)$$

where ECO, EPH, ESR, α_1 and $\mu 0$ are adjustable parameters, and E_{eff} the vertical electrical field in the inversion layer, which is a function of the inversion charge Q_i and of the bulk charge Q_b:

$$E_{eff} = \frac{q\left(\eta Q_i + Q_b\right)}{\varepsilon_{Si}} \quad (2)$$

with η = 1/2 for NMOS and 1/3 for PMOS.

The relationship among charges and applied biases is provided by the charge-voltage relationship provided by the EKV model [1] valid at all levels of inversion. The vertical field mobility model is also combined with a charge-based expression for the effect of velocity saturation, extending the application to short-channel as well, where the critical field UCRIT is a (temperature dependent) model parameter. Unlike common MOSFET models, the present model accounts for position- (and bias-) dependence of mobility through the MOS channel.
The mobility model is therefore fully consistent with the basic charge model approach. The resulting compact model is overall very coherent as well as continuous in all operating regions, from weak to strong inversion and from triode to saturation.
Further specific features, such as improved accounting for weak inversion slope degradation, completed the present specific low-temperature extensions of the EKV model.
The full model was implemented in the ELDO® circuit simulator from Mentor Graphics as a proprietary model using the User Defined Model (UDM/CMPI) interface. It was also implemented in the Silvaco UTMOST® software used for device parameters extraction and optimisation.

The improved charge-based mobility model allows to reproduce accurately the drain current both in the ohmic mode (|Vds| = 50 mV) and in the saturation mode (|Vds| = 2.5 V) as seen in Fig. 1, 2 for NMOS transistors and in Fig. 3, 4 for PMOS transistors. It allows also to reproduce accurately the gate transconductance (Gm) which could be even negative on NMOS transistors in the ohmic mode at high vertical fields (Fig. 5). A good agreement between measurement and simulation is also found on short-channel transistors as illustrated in Fig. 6, 7. The simulated characteristics in these figures were obtained after optimisation on different MOSFETs with drawn length down to 0.21 µm and drawn width down to 0.6 µm.

The mobility in short-channel transistors, particularly for NMOS, is strongly affected by velocity saturation of the carriers, limiting the total available drain current. Figure 8 shows the evolution of the saturation drain current at 77 K relative to its value at 293 K for NMOS and PMOS devices with channel length. As can be seen from the figure, while this ratio is 3 and 1.9 at long channel, it drops to 1.4 and 1.2 at short channel, for NMOS and PMOS transistors, respectively. This indirectly illustrates the importance of velocity saturation which remains one of the main effects limiting short-channel device performance at low temperature.

As this deep submicron CMOS technology has pocket implants, we observe an important increase of the drain conductance (Gds) in saturation on long channel transistors [5,6]. Since this effect is not yet modeled in the framework of the EKV 2.6 model, two sets of parameters needed to be extracted: a first one for drawn length covering 0.21 and 0.5 µm and a second one for greater length.

In the previously studied 0.35 µm CMOS processes, a carrier freeze-out effect was observed in the LDD zones at temperatures lower than 150 K leading to an important error when evaluating the drain conductance of short transistors at very low drain-to-source voltages (less than 250 mV) in strong inversion. Although LDD zones also exist in the present 0.21 µm process, we did not observe any freeze-out effects down to 77 K.

LOW FREQUENCY NOISE PARAMETERS

Flicker noise parameters were extracted on this technology using the following model:

$$S_{Id} = \frac{KF\, G_m^2}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \quad (3)$$

For analog application, special emphasis was placed on extracting the AF and KF noise parameters in the weak and moderate inversion regimes. Noise measurements were done in saturation (|Vds| = 1.8 V) on different devices with length varying between 0.21 and 20 µm and width between 1.4 and 20 µm. Noise spectral densities measured at different gate transconductance (Gm) were then optimised. The evolution of the flicker noise parameter KF with temperature obtained after optimisation in weak-moderate inversion is shown in Fig. 9. Contrary to NMOS transistors, the KF parameter of PMOS transistors decreases with temperature.

The preceding flicker noise model was also tested at room temperature and at 77 K in a wider range of gate transconductance covering also the strong inversion regime (Fig. 10, 11). We experimentally found that a better agreement with measurements would be obtained by modifying relation (3) according to:

$$S_{Id} = \frac{KF\, G_m^{EF}}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \quad (4)$$

where EF is a process-dependent exponent, not strictly equal to 2, allowing to reproduce the bias dependence (see Ref. [7] and references therein) of input referred noise voltage S_{Id} / Gm^2. The EF parameter values we measure for NMOS and PMOS transistors from different 0.5, 0.35 and 0.21 µm technologies at low temperature or at room temperature lie between 1.8 and 2.3.

SUMMARY

A specific model based on the EKV 2.6 compact MOSFET model was successfully applied for parameter extraction and simulation at low temperature of analog circuits on different submicron CMOS processes from different foundries. New model features, in particular an evolved mobility model and improved accounting for weak inversion slope degradation, allow this model to be successfully applied in all inversion regimes and over different geometries and temperatures. The model's performance has been demonstrated in this paper for a 0.21 µm dual polysilicon gate technology with pocket implants. The pocket implants degrade the output conductance even in long-channel devices, requiring the model to be binned over different geometries. Further R&D is required to fully address this effect in terms of modeling.

Experimental results on the evolution of the low-frequency noise parameters at low temperature down to 77 K for both NMOS and PMOS transistors have also been presented. For PMOS transistors, a decrease of the KF parameter – independently whether a buried channel is used or not – could be found experimentally when lowering the temperature, contrary to the increase found in NMOS transistors.

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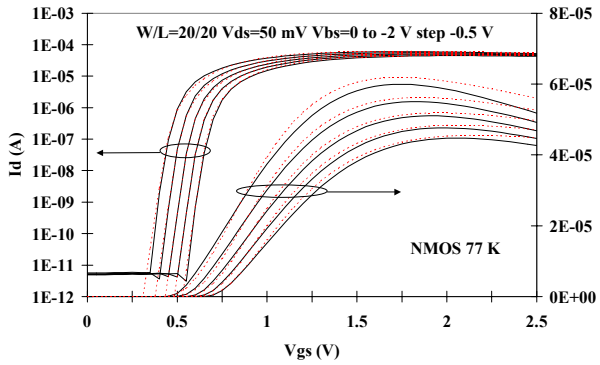

Fig. 1 Measured (—) and simulated (...) NMOS drain current with the EKV/LT model: linear regime.

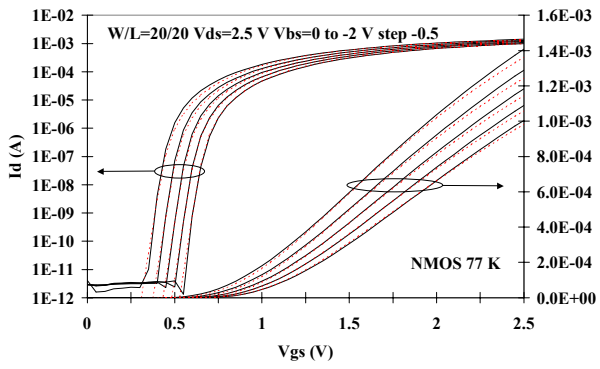

Fig. 2 Measured (—) and simulated (...) NMOS drain current with the EKV/LT model: saturation regime.

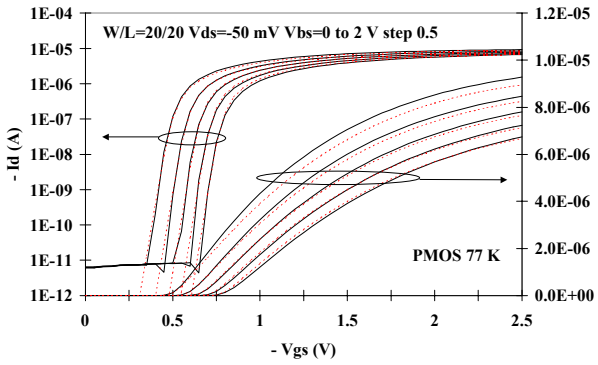

Fig. 3 Measured (—) and simulated (...) PMOS drain current: linear regime.

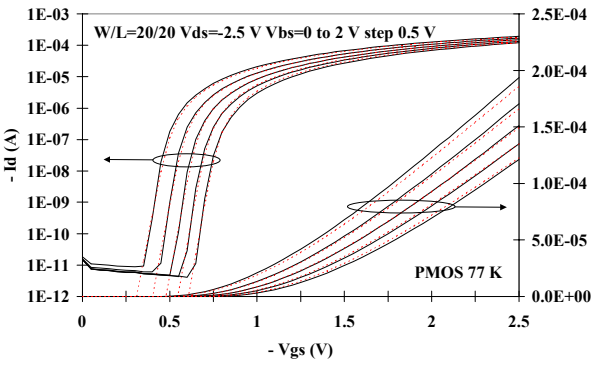

Fig. 4 Measured (—) and simulated (...) PMOS drain current: saturation regime.

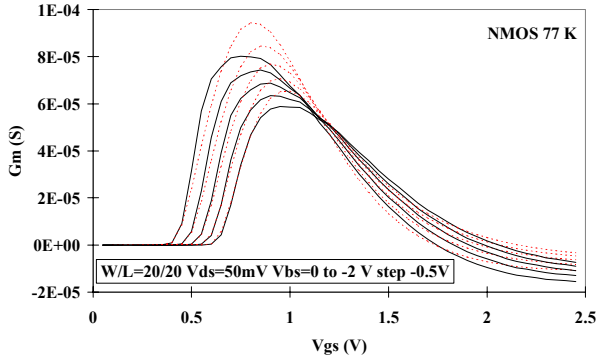

Fig. 5 Measured (—) and simulated (...) NMOS gate transconductance in the linear regime at 77 K.

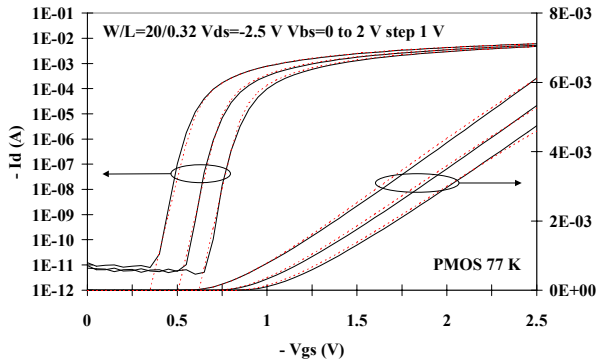

Fig. 6 Measured (—) and simulated (...) Id - Vgs characteristics for a short-channel PMOS.

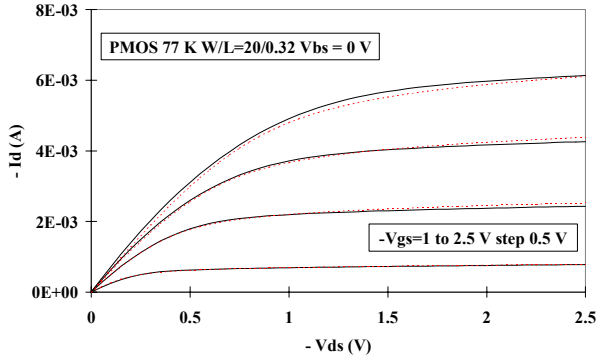

Fig. 7 Measured (—) and simulated (...) Id - Vds characteristics for a short-channel PMOS.

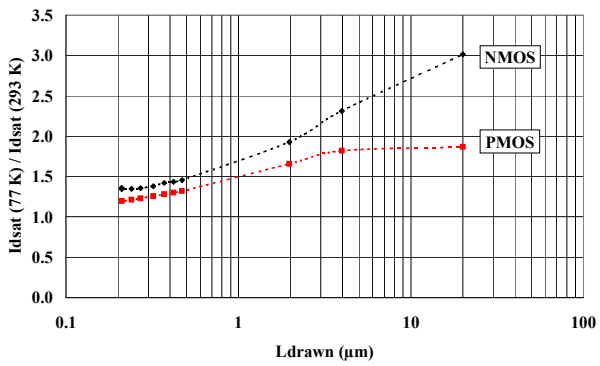

Fig. 8 Ratio of saturation drain current at 77 K and 293 K versus the drawn length for NMOS and PMOS transistors (|Vds|=|Vgs|=2.5 V)

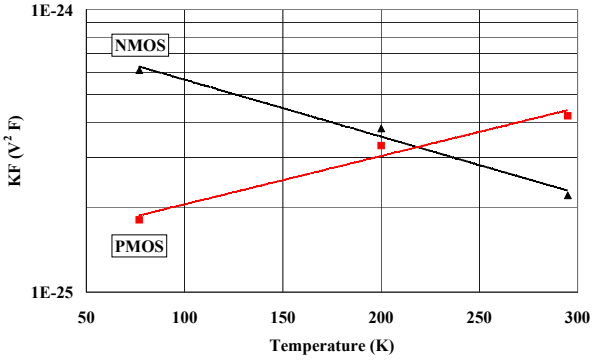

Fig. 9 Evolution of the flicker noise parameter KF with temperature using eq. (3). From measurements in weak-moderate inversion (Gm NMOS(PMOS) < 60(10) µS at 77 K)

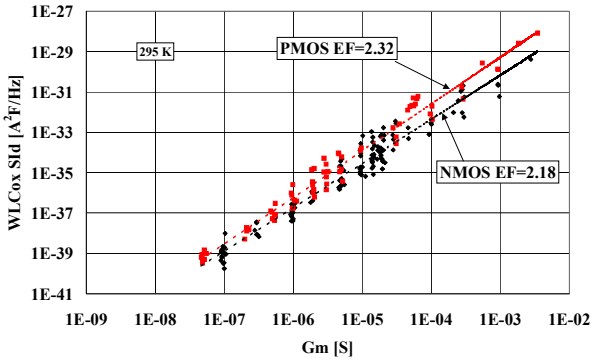

Fig. 10 Flicker noise model at 295 K (|Vds|=1.8 V, f = 1 Hz, Tox=3.9 nm, Cox=8.85 10^{-3} F/m^2).

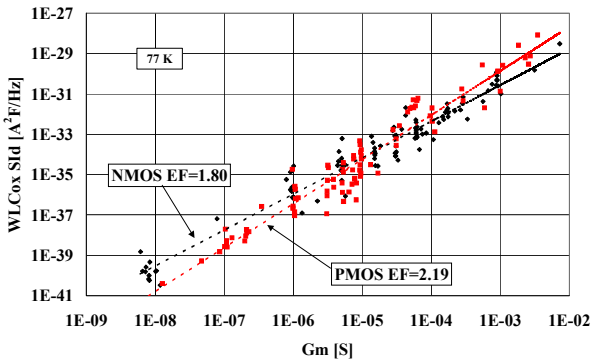

Fig. 11 Flicker noise at 77 K (same devices and bias conditions as in Fig. 10).