J. Phys. IV France **12** (2002)
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DOI 10.1051/jp420020035

MOSFET modeling and parameter extraction for low temperature analog circuit design

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Abstract: SPICE parameters needed for simulation of CMOS readout circuits used in infrared image sensors cooled at low temperature are extracted using a specific MOSFET model based on the EKV 2.6 compact charge model It is used below 200 K and is very well adapted to analog simulation in weak and moderate inversion regimes It was successively applied on different CMOS processes from different foundries. The model's performance is demonstrated in this work for a 0.35 μm N^+ single gate process Experimental results on the evolution of the low frequency noise and the transistor matching parameters between 300 K and 77 K are also presented Contrary to the NMOS transistors, the threshold voltage differences of buried channel PMOS transistors are less scattered as the temperature is lowered The same trend with temperature is observed on the flicker noise parameter

1. INTRODUCTION

SPICE parameters are needed for simulation and design of CMOS readout circuits used in infrared focal plane arrays (IRFPA) working at low (77 K) or at intermediate temperature (130 K, 200 K). As CMOS foundries do not provide them, full sets of MOSFET parameters (DC, AC, 1/f noise and matching parameters) must be extracted prior to circuit simulation using a MOSFET model placing special emphasis on the weak and moderate inversion regimes where most of the transistors of the IRCMOS readout circuits are operating. In this paper we use a specific model based on the EKV 2.6 compact charge model formalism [1] and developed in collaboration with the EPFL modeling group [2]. It was successively applied on different stabilized CMOS bulk processes such as 0.7 μm-5 V [3], 0.5 and 0.35 μm-3.3 V, with and without dual polysilicon gates, from different foundries. The model's performance is demonstrated in this paper for a 0.35 μm N^+ gate technology. Experimental results on the evolution of the low frequency noise and transistor matching parameters down to 77 K for both NMOS and PMOS transistors are also presented.

2. THE LOW TEMPERATURE VERSION OF THE EKV 2.6 MODEL

The standard EKV 2.6 model [1] from EPFL, as well as for most MOSFET models including BSIM3v3 of University of California, Berkeley, is valid at or near room temperature. As soon as the temperature is lower than 200 K, the EKV 2.6 model is unable to reproduce accurately the experimental electrical characteristics. A modified model has then to be used due to physical phenomena specific to low temperature.

In particular this model incorporates a new charge-based mobility model for low temperature application including Coulomb, phonon and surface roughness scattering mechanisms as well as velocity saturation. The mobility law for the effective vertical field is given by:

$$\mu = \frac{\mu_0}{\left(\frac{E_{eff}}{ECO}\right)^{\alpha_1} + \left(\frac{E_{eff}}{EPH}\right)^{1/\alpha_1} + \left(\frac{E_{eff}}{ESR}\right)^2} \quad (1)$$

where ECO, EPH, ESR, α_1 and $\mu 0$ are adjustable parameters, and E_{eff} the vertical electrical field in the inversion layer which is a function of the inversion charge Q_i and of the bulk charge Q_b:

$$E_{eff} = \frac{q\,(\eta\, Q_i + Q_b)}{\varepsilon_{Si}} \quad (2)$$

with η = 1/2 for NMOS and 1/3 for PMOS.

The effective mobility of the whole channel is obtained via integration of the above local mobility law along the channel. Therefore, the vertical field dependent effective mobility becomes itself dependent on the field along the channel. The effect of velocity saturation on mobility is also introduced in a similar manner. No additional parameters for bias dependence with substrate or drain effects need to be introduced in the mobility model.

The implementation of this charge-based mobility model is a major improvement as it allows to reproduce very accurately the drain current as seen in Fig. 1 and Fig. 2. The fitting of the gate transconductance Gm, which is the most difficult test for the mobility model in the ohmic mode, is also presented.

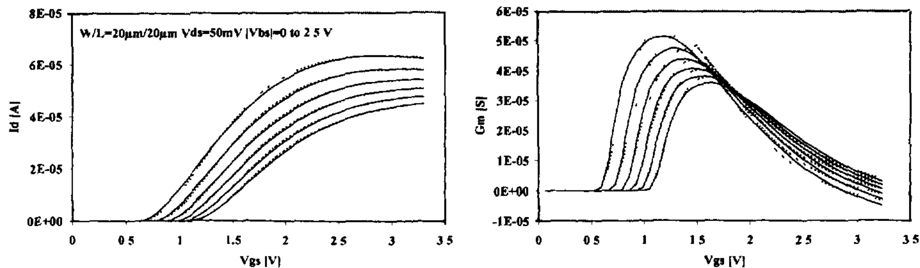

Figure 1 Measured (—) and simulated ( ) NMOS drain current and gate transconductance with the EKV/LT model at 77 K in the ohmic mode

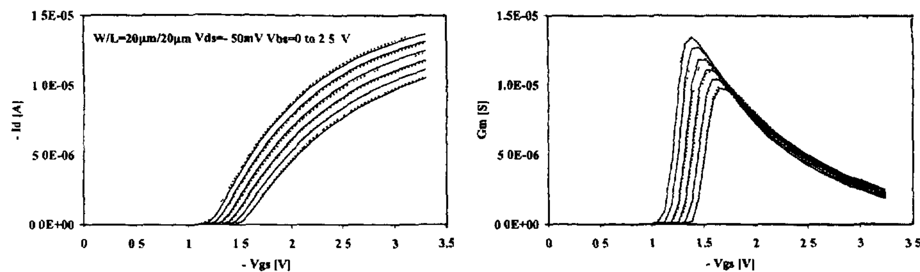

Figure 2 Measured (—) and simulated ( ) PMOS drain current and gate transconductance at 77 K

The measured and simulated drain current and conductance Gds in weak to moderate inversion are plotted in Fig. 3 and Fig. 4. The conductance is presented in logarithmic axes in order to show the continuous transition between ohmic and saturation modes and the satisfying agreement between simulation and measurement even for extremely small output conductances.

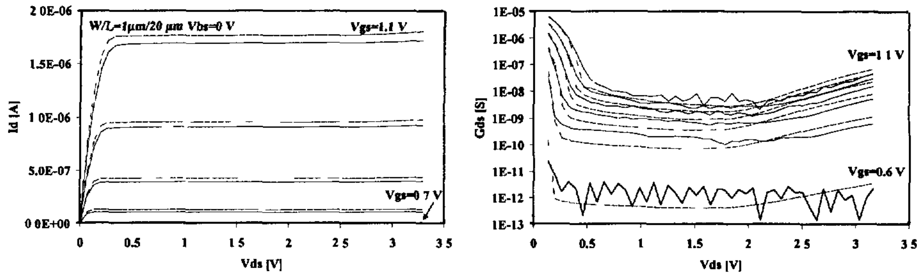

Figure 3 Measured (—) and simulated (.) NMOS drain current and conductance in weak to moderate inversion at 77 K

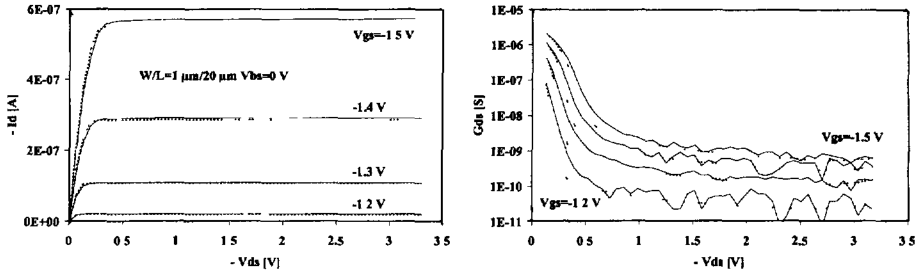

Figure 4. Measured (—) and simulated (..) PMOS drain current and conductance in weak to moderate inversion at 77 K

Depending on the CMOS technology, PMOS transistors can experience surface conduction (P^+ doped polysilicon gate in a dual process) or volume conduction (N^+ doped gate) In this latter case, some freeze-out effects arise at temperature lower than 200 K. As a consequence, the subthreshold swing is degraded compared to NMOS for which the subthreshold swing is 21 mV/decade at 77 K. This phenomenon is complex as it depends not only on the temperature but also on the bias and the geometry. It cannot be formulated precisely in a compact model needed by a circuit simulator However, as a first approximation, this effect is taken into account in the low temperature version of the EKV model by introducing a new parameter (NUO $\geq$ 1) such that the weak inversion slope may excess its theoretical value depending only on the temperature (NUO = 1). This parameter allows minimising the error in weak inversion as illustrated in Fig. 5, but does not affect the strong inversion regime [4].

Another phenomenon which appears at temperatures around 150 K for NMOS transistors in this technology is the carrier freeze-out effect in the LDD zones. This effect is also complex and is not taken into account. As a result, an error exists when evaluating the drain conductance of short transistors at low drain-to-source voltages (less than 250 mV) where this effect is the most severe (Fig. 6). However, this phenomenon is no more of importance in saturation due to a field-assisted impurity ionisation effect as described in Ref. [5].

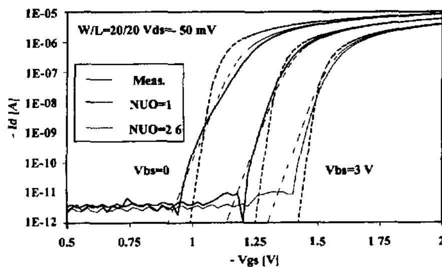

Figure 5 Buried channel freeze-out effects in PMOS transistors at 77 K.

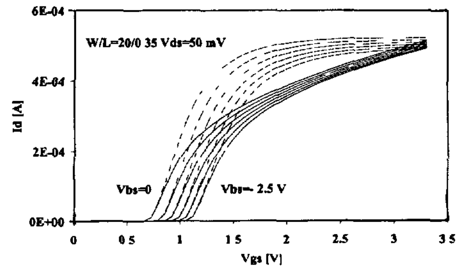

Figure 6 Freeze-out effects in LDD zones for a short NMOS transistor at 77 K

This charge-based and still compact model is valid and continuous in all operating regions, from weak to strong inversion and from triode to saturation. It was implemented in the ELDO® circuit simulator from Mentor Graphics as a proprietary model using the User Defined Model (UDM/CMPI) interface. It was also implemented in the Silvaco UTMOST® software used for device parameters extraction and optimisation.

3. LOW FREQUENCY NOISE PARAMETERS

Flicker noise parameters were extracted on this technology at 77 K, 200 K and 300 K using the following model:

$$S_{Id} = \frac{KF\, G_m^2}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \quad (3)$$

For analog application, special emphasis was placed on extracting the AF and KF noise parameters in the weak and moderate inversion regimes. The evolution of the flicker noise parameter KF with temperature is shown in Fig. 7 Contrary to NMOS transistors, the KF parameter of PMOS transistors decreases with temperature.

The preceding flicker noise model was also tested at 300 K and 77 K in a wide range of gate transconductance covering weak, moderate and strong inversion regimes for both NMOS and PMOS transistors (Fig. 8). We experimentally found that a better agreement with measurements would be obtained by modifying relation (3) according to:

$$S_{Id} = \frac{KF\, G_m^{EF}}{C_{ox}\, W_{eff}\, L_{eff}\, f^{AF}} \quad (4)$$

where EF is a process-dependent exponent, not strictly equal to 2, and allowing to explain why the input gate referred noise voltage S_{Id} / Gm^2 is generally not bias-independent as pointed out by different authors (Ref. [6] and references therein). The EF parameter values we measure for NMOS and PMOS transistors from different 0.5 and 0.35 µm technologies at low temperature or at room temperature lie between 1.8 and 2.3.

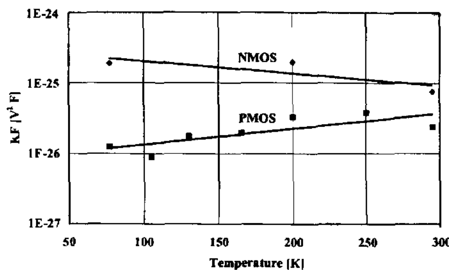

Figure 7 Evolution of the flicker noise parameter KF with temperature

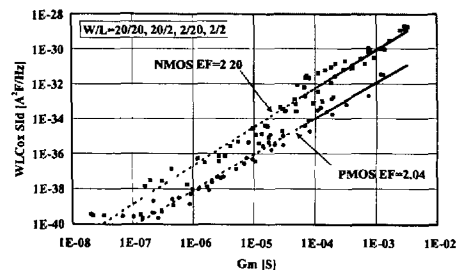

Figure 8. Test of the flicker noise model at 77 K (0 35 µm N+ gate process, |Vds|=3 V, f = 1 Hz)

4. MATCHING PARAMETERS

The EKV 2.6 model [1] as well as in its evolved version presented here, has a built-in ability to account for geometry- and bias-dependent device-to-device matching in statistical circuit analysis using a single

model parameter set per device type. Note that such a feature is not commonly available with other MOSFET models.

The matching parameters were extracted on this 0.35 μm CMOS process using dedicated test structures containing a number of modules for NMOS and PMOS transistors with different sizes (W x L =12.6x12.6, 12.6x1.75, 0.77x12.6, 1.75x1.75, 0.77x0.77 and 0.49x0.35 μm^2) Each module has 21 transistors of the same size, placed in line and spaced by 14 μm. The measurements reported in this paper were made by extracting the parameters in the linear mode. Measured matching parameters at different temperature for the threshold voltage (VTO), current factor (KP) and substrate coefficient (GAMMA) using equation (5) from Ref. 7 are given in Fig. 9, 10 and 11. No variation of the mismatch with the spacing (D) between pairs was experimentally found on this stabilized process. To the knowledge of the authors, such matching data at low temperature and their evolution with temperature are very scarce in the literature.

$$\sigma^2(\Delta P)=\frac{A_P^2}{WL}+S_P^2 D^2 \quad (5)$$

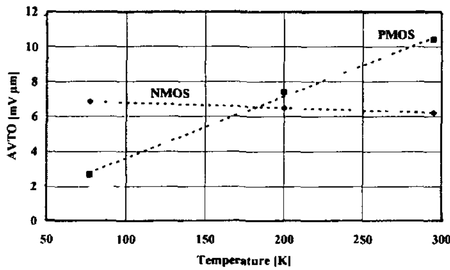

Figure 9 Evolution of the AVTO mismatch parameter with temperature (Tox = 7 5 nm)

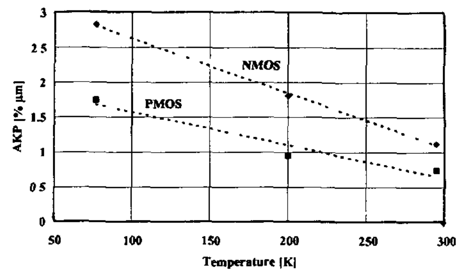

Figure 10. Evolution of the AKP mismatch parameter with temperature

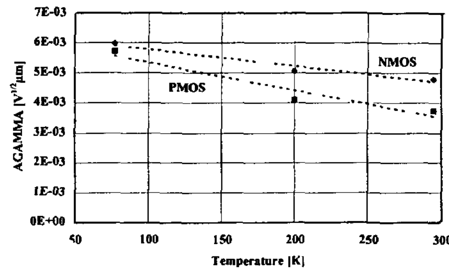

Figure 11 Evolution of the AGAMMA mismatch parameter with temperature

As a general rule, transistor matching is poorer at low temperature. The notable exception is the threshold voltage mismatch parameter for the buried PMOS transistors of this process, which decreases with temperature and is very low at 77 K. We have already observed the same behaviour on PMOS transistors from a 0.7 μm N^+ gate process [3] where the LF noise was also found to decrease with temperature. There is probably a correlation between the improvement in both LF noise and threshold voltage mismatch for these buried channel PMOS transistors possibly due to the decreased incidence of interface states.

The standard deviation of the drain current for the different modules was also measured in saturation (|Vds|=3.3 V) for several gate-to-source voltages, from weak to strong inversion. This deviation has been found to be well reproduced in all inversion regimes and geometries by the simulation model using the full matching simulation capability and extracted matching parameters (Fig. 12).

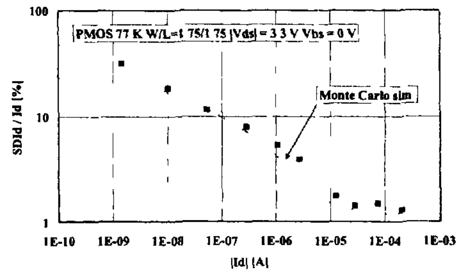

Figure 12. Measured and simulated drain current mismatch in saturation from weak to strong inversion.

5. SUMMARY

A specific model based on the EKV 2.6 compact model was successfully applied for parameter extraction and simulation at low temperature of analog circuits on different submicron CMOS processes from different foundries. Additional model features, in particular an evolved mobility model and improved modeling of weak inversion slope degradation, allow this model to be successfully applied in all inversion regimes and over different geometries and temperatures. The model's performance has been demonstrated in this paper for a 0.35 µm N^+ single gate technology. Experimental results on the evolution of the low frequency noise and transistor matching parameters at low temperature down to 77 K for both NMOS and PMOS transistors have also been presented. We experimentally found that contrary to the NMOS transistors, the threshold voltage differences of buried channel PMOS transistors are less scattered as the temperature is lowered. The same trend with temperature is observed on the KF flicker noise parameter. With the present extensions, the EKV MOSFET model, combined with specific parameter extraction, proves to be an excellent tool to support analog CMOS IC design at low temperatures. The simulation capabilities for matching and noise, including weak and moderate inversion, are particularly appreciated. This model is now being tested on a 0.21 µm-1.8 V process.

Acknowledgements

The authors would like to thank C. Chancel for experimental support. This work was supported in part by DGA/DTCO.

References

[1] M. Bucher, C. Lallement, C. Enz, F. Théodoloz and F. Krummenacher. The EPFL-EKV MOSFET model equations for simulation, version 2.6, EPFL Tech. Rep. (1997) [http://legwww.epfl.ch/ekv/].

[2] F Théodoloz, C. Enz and M. Bucher, "Charge Based MOS Transistor Mobility Modeling Applicable at Low Temperature", unpublished EPFL technical report (1999).

[3] P. Castelein, P. Audebert and P. Martin, " IRFPA advanced behavioural modeling dedicated to optronic systems evaluations", in Proc. SPIE 15th International Symposium on AeroSense, Aerospace/Defense Sensing, Simulation and Controls, Orlando, 2001

[4] M. Bucher, "Analytical MOS Transistor Modeling for Analog Circuit Simulation", Ph. D. Thesis 2114, EPFL, Lausanne, Switzerland, 1999.

[5] I.M. Hafez, G. Ghibaudo, F. Balestra, and M. Haond, "Impact of LDD Structures on the Operation of Silicon MOSFET's at Low Temperature", Solid-State Electronics, vol. 38, no 2 (1995) pp. 419-424.

[6] E.P. Vandamme and L.K.J. Vandamme, "Critical Discussion on Unified 1/f Noise Models for MOSFETs", IEEE Trans. Electron Devices, vol. 47, no 11 (2000) pp. 2146-2152.

[7] M.J.M. Pelgrom, A.C.J. Duinmaijer and A.P.G. Welbers, "Matching Properties of MOS Transistors", IEEE Journal of Solid-State Circuits, vol. 24, no 5 (1989) pp. 1433-1440.